

Power Optimized Voltage Level Shifter Design for High Speed Dual Supply Application

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Abstract – Reduction of power consumption has always been major design goal in energy harvesting digital devices. One effective way for low power design use of multiple voltages depends on their speed. This, however, accomplish the use of interface block called level converters or level shifters. This paper presents a modified structure of level shifter for lower power implementation. Simulation results of proposed structure in a 0.18-um CMOS technology show that the design of input low supply voltage of 0.4V and high supply voltage of 1.8V, the level shifter has a propagation delay of 12.5ns and a power dissipation of 87.7nW for a 1-MHz input signal. Then comparison is done against these level shifters in terms of power, speed and power delay product.

Key Words: CMOS, level converter, subthreshold operation, Dual supply circuits, power delay product.

1. INTRODUCTION

Power efficiency and speed are major factor of performance in all digital circuits. Various techniques have used to reduce dynamic and static power. On the other hand, reducing the supply voltage increases the propagation delay of the circuits [2]. In order to avoid these problems dual supply architecture are introduced in which a low voltage (V_{ddL}) is supplied for the blocks on the noncritical paths while a high supply voltage (V_{ddH}) is applied to the analog and the high-speed digital blocks. Some of the most commonly used techniques are dynamic voltage scaling operating down to near threshold voltage levels and supporting multiple voltage domains. That is why Level shifting circuit is needed to provide exact voltage level for the circuit. A voltage level shifter is one of the major components in a digital system. Level shifters are used for provide correct voltage level for each component in the digital circuits.

A wide variety of level shifters have been proposed in the literature review. Designers move their attention to implement a voltage level shifter, which operates minimum power consumption and maximum speed. Moreover the level shifter must able to operate correctly for subthreshold input signals. Some of the recently reported high performance voltage level shifters are reviewed. The proposed circuit introduced in section 3. Section 4 presents the simulation result of the modified circuit verifying the efficiency of the proposed circuit. Finally, concluded in section 5.

Circuit designers are faced with the challenge of developing systems with increasing functionality and complexity while under demanding power and time-to-market constraints. Such systems often require voltage level translation devices to allow interfacing between integrated circuit devices built from different process technologies. The choice of the proper voltage level translation device depends on many factors and will affect the performance and efficiency of the circuit application. Thus voltage level shifters play an important role in widely used VLSI systems.

Voltage level translation is needed when two devices have differing supply voltage nodes. Two possible conditions exist. A higher-voltage device may be needed to drive a low-voltage device. A lower-voltage device may be needed to drive a high-voltage device.

If the low voltage device is the driver, the circuit typically cannot function properly without the use of a translation device.

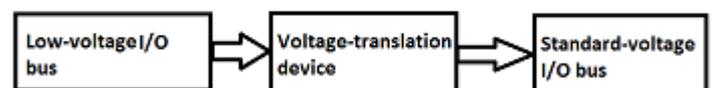


Fig-1: Voltage levelshifter functioning

2. EXISTING LEVEL SHIFTER IMPLEMENTATION

In this section, circuit configuration and advantages of two level converters recently reported will be briefly explained. The operation of the circuit shown in Fig.2, is as follows. When the input signal becomes high transistor M_{n1} turns on and nmos transistor M_{n4} turns on because the overdrive voltage of M_{p3} larger than the M_{n3} . Therefore transition current flows M_{p1} , M_{n1} , and M_{n4} and this current is mirrored to M_{p2} and tries to pull up the output node. Finally the output is pulled up and the transistor M_{p3} turned off consequently nmos transistor M_{n4} pull down by the nmos transistor M_{n3} , means no static current flows through M_{p1} , M_{n1} , and M_{n4} .

If the input is low and INB is high, the nmos transistor M_{n2} conducts and pulls down the output node at the same time nmos transistor M_{n1} off and no static current flows. This means that current of M_{p2} is not completely close to zero weak contention exist. Further reduce the value of current another device M_{p4} is used.

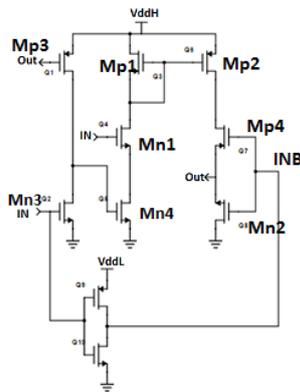


Fig-1: Circuit diagram of voltage level shifter [1]

2.1 EXTENSION OF LEVEL SHIFTER WITH AUXILIARY CIRCUIT

In order to further reduction of power and delay as an extension of voltage level shifter with auxiliary circuit is used, shown in Fig.2. Auxiliary circuit turns only high to low transition of input signal and to pull up the node Qc to a value larger than VddL.

Transistor Mn6, Mn7 and Mp6 are turned on and nmos transistor Mn5 turned off, therefore transition current flows through Mn6, Mn7, Mp6 are mirrors to Mp7 and pull up the node Qc.

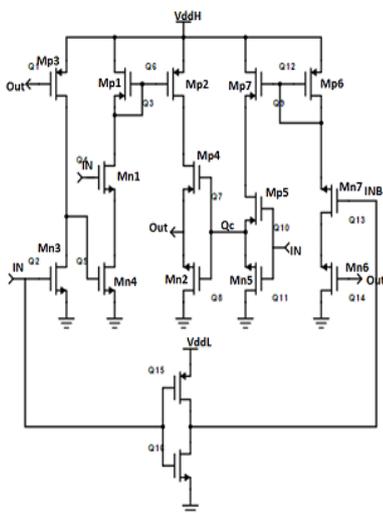


Fig -2: Extension of voltage level shifter with auxiliary circuit [1]

The strength of pull-up devices is significantly reduced when the pull down device is pulling down the output node, but the strength of pull down device is also increased using a low power auxiliary circuit.

3. PROPOSED VOLTAGE LEVEL SHIFTER CIRCUIT

A new power optimized proposed voltage level shifter is introduced. Here the power gating technology is implemented for power optimization.

Power gating is the circuit design technique that has been most widely used in industrial products, means connecting sleep transistor to combination of pull up pull down network to reduce the subthreshold leakage current. A sleep transistor is separating the pull up network from Vdd and pull down network from Vss.

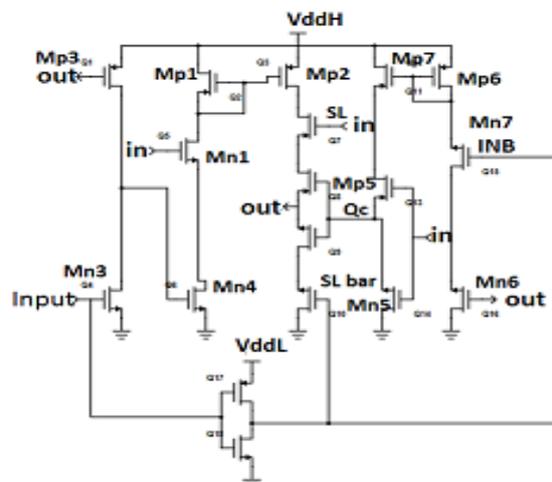


Fig-3: Proposed Voltage level shifter

Sleep transistor SL separates transistor Mp4 from Vdd and SL bar separates nmos transistor Mn5 from Vss. During active mode SL=0, sleep transistor turns on and provide low resistance in the conduction path. Circuit cut off from its power supply in sleep mode SL=1 by means of current switch.

4. SIMULATION RESULTS

The voltage level shifter design in fig.1 was implemented in 180 nm by using cadence virtuoso software. Then the transient analysis is obtained as in fig.5.

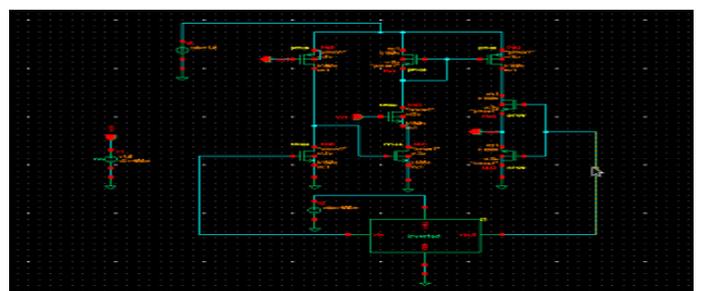


Fig-4: Implementation of voltage level shifter

The power consumption of voltage level shifter can be classified in two static power consumption and dynamic power consumption. Static power dissipation caused from

leakage current in the CMOS based integrated circuits. Leakage power is minimized only in standby mode. This is lower than dynamic power dissipation, which arises due to charging and discharging of load capacitance. For 180 nm technology the total power consumption of the voltage level shifter was found to be 172.9nW. Delay of voltage level shifter was found to be 62.1ns.

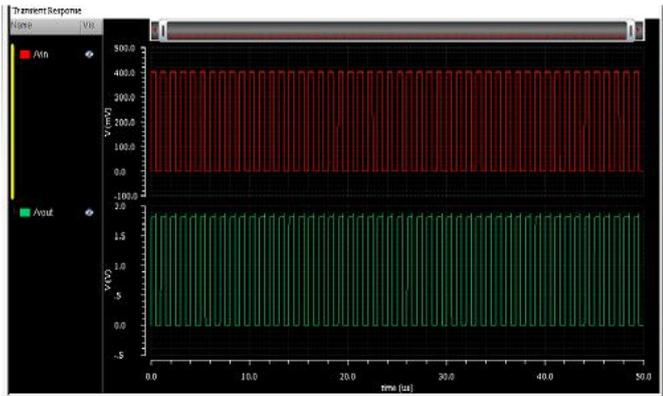


Fig-5: Transient analysis of voltage level shifter

In order to further reduction of power and delay as an extension of voltage level shifter with auxiliary circuit is used [1]. Level shifter with auxiliary circuit was implemented in fig-6 and power and delay calculated.

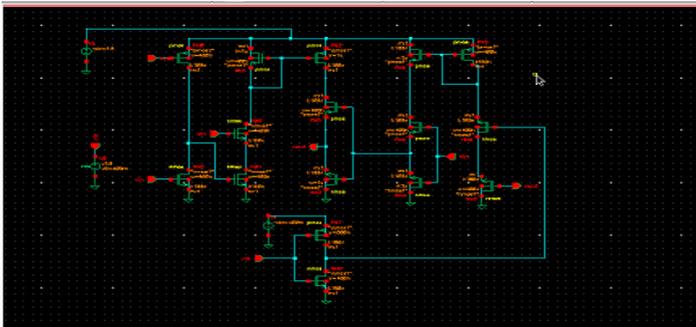


FIG-6: Extension of Level shifter with Auxiliary circuit

Power and delay of level shifter with auxiliary circuit was found to be 166.01nW and 12.1ns respectively. The simulation was done in 180nm technology by cadence virtuoso software.

The new proposed power optimized voltage level shifter was implemented in fig-6. The average power consumption was found to be 87.57nW. Power is reduced to 50% compared to other level shifter designs. The leakage power was compressed by power gating technology.

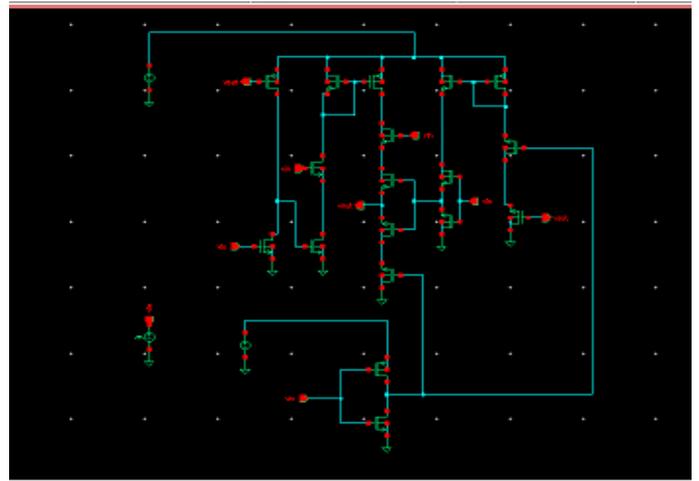


FIG-7: Implementation of Proposed Voltage Level Shifter

The simulation results were compared in table: 1.

Table-1: Comparison Results of Voltage Level shifters

Designs(180nm)	Average power(nW)	Delay(ns)	Power Delay Product (nW.ns)
Existing voltage level Shifter	172.9nW	62.1ns	10737.09
Level Shifter with Auxiliary circuit	166.01nW	12.1ns	2008.721
Proposed Voltage Level Shifter	87.57nW	12.5ns	1094.625

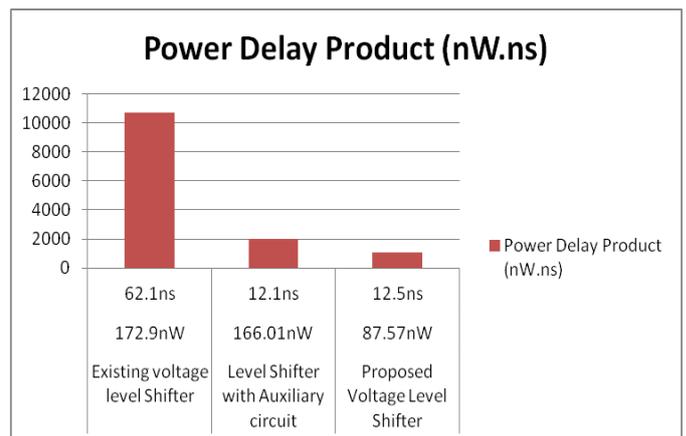


Chart-1: Bar Diagram Representation of Simulation Result

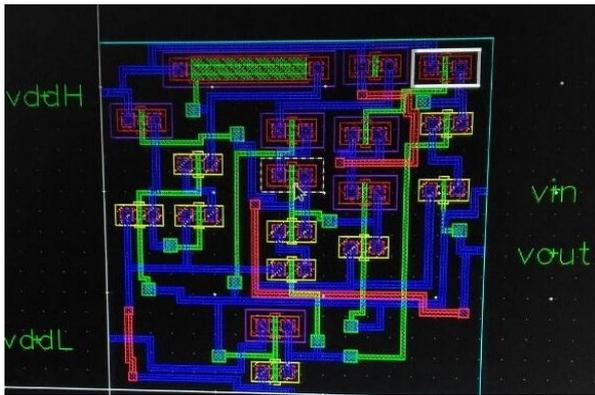


Fig-8: Layout implementation of proposed voltage level shifter

- [8] A.Wang and A. P. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 310–319, Jan. 2005.

6. CONCLUSION

In this brief, a fast and low power voltage level shifting design was proposed which is able to convert extremely low values of input voltages. Both existing and proposed designs were simulated using cadence virtuoso tools. Average power dissipation of the proposed design was reduced to half as compared to existing voltage level shifter. The average power dissipation was found to be 87.5nW. PDP of both designs are measured and it is observed to be minimum in the case of proposed design.

REFERENCES

- [1] Seyed Rasool Hosseini, Mehdi Saberi, and Reza Lotfi A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications Oct. 2016.
- [2] S. Rasool Hosseini, Mehdi Saberi and Reza Lotfi, "A Low-Power Subthreshold to Above-Threshold Voltage Level Shifter", *IEEE Trans. Circuits Syst. II*, vol. 61, no. 10, pp. 753–757, Oct. 2014.
- [3] H. Shao and C.-Y. Tsui, "A robust, input voltage adaptive and low energy consumption level converter for sub-threshold logic," in *Proc. IEEE ESSCIRC*, 2007, pp. 312–315.
- [4] S. Lütkemeier and U. Rückert, "A subthreshold to above-threshold level shifter comprising a Wilson current mirror," *IEEE Trans. Circuits Syst. II*, vol. 57, no. 9, pp. 721–724, Sep. 2010.
- [5] M. Lanuzza, P. Corsonello, and S. Perri, "Fast and wide range voltage conversion in multisupply voltage designs," *IEEE Trans. Very Large scale Integr. (VLSI) Syst.*, vol. 23, no. 2, pp. 388–391, Feb. 2015.
- [6] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1776–1783, Jul. 2012.
- [7] K. Usami *et al.*, "Automated low-power technique exploiting multiple supply voltages applied to a media processor," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 463–472, Mar. 1998.