International Research Journal of Engineering and Technology (IRJET)e-ISSN: 2395 -0056Volume: 04 Issue: 04 | Apr -2017www.irjet.netp-ISSN: 2395-0072

Efficient Design Of Variable Length Fourier Transform For Digital Broadcasting

Sheetal Arvind Kolte , Professor Vinay keswani, Prof.Nilesh Bodne

¹Department Of ECE ,Vidarbha Institute Of Technology College Of Engineering Nagpur, India ^{2,3} Professor ,Department Of ECE, Vidarbha Institute Of Technology College Of Engineering Nagpur, India

______***______***______

Abstract— The focus of this paper is on a fast implementation of the DFT called the FFT (Fast Fourier Transform) and the IFFT (Inverse Fast Fourier Transform). The implementation is based on a well known algorithm, called the split Radix FFT., . This is split radix which is combination of radix 2 and radix 4 fast fourier transform to effectively compute the variable-length Fourier transform (VLFT) by reducing number of multiplication and addition which are in fast fourier transform

Keywords- FFT (Fast Fourier Transform), IFFT (Inverse Fast Fourier Transform), VLFT (variable-length Fourier transform, DFT,(discrete fourier transform), OFDM (Orthogonal Frequency Division Multiplexing)

1. INTRODUCTION AND MOTIVATION

A fast Fourier Transform (ffT) processor is one of the major components of an Orthogonal Frequency Division Multiplexing (OFDM) communication systemThis algorithm has been widely adopted in digital signal processing and multimedia applications so as to to reduse the calculation of transferring the signal. With the wides pread utilization of FFT, many techniques and method have been introduce to speed up the FFT algorithm in recent yea in both wired and wireless communication. To achieve the minimum throughput requirement of the different standards on a less power hungry so to achive such we requires a highly optimized design to do so. So in our paper we are introducing the split radix which reduces the n-number of multiplication and addition and reduces time in fourier transform.

VLFT plays an important role in the orthogonal frequency division multiplexing (OFDM) communication systems. where a single device integrates various wired and wireless communication standard suchas, Digital Audio Broadcasting (DAB),Very high speed Digital Subscriber Loop (VDSL),, and it is applicable to all useful fFT processor lengths such as 512/1,024/2,048/4,096/8,192 points can used in OFDMbased communication systems. Although the performance of FFT on recent computer hardware is determined by many factors besides pure arithmetic counts. in feature if the more deep studyand a great convervation would held and take the review from expert we wil have refine the proposed solution to minimize power consumption

2. DERAVATION FOR FFT

This section describes the mathematical basis and some FFT algorithms which are applied to develop our VL-FFT processor. An N-point discrete Fourier transform of a sequence x[n]is given as $X[k] = \sum_{n=1}^{N-1} x[n] W_N^{nk}$ where k = 0, 1, 2, ... Ntwiddle where the factor $W_N = e^{\frac{-j 2 \pi}{N}} = co \, s \left(\frac{2 \pi}{N} \right) - j sin(\frac{2 \pi}{N})$. In general, FFT algorithms are derived by taking advantage of the symmetry properties of twiddle factor as shown in Fig. 1.



Figure 1. The twiddle-factor of an N-point DFT.

The split-radix algorithm is proposed by mixing the <u>radix-</u>2 and <u>radix-4</u> equation.

$$\begin{split} X(k) &= \sum N2 - 1n = 0x(2n)e - (i2\pi \times (2n)kN) + \sum N4 - 1n = 0x(4n+1)\\ e - (i2\pi(4n+1)kN) + \sum N4 - 1n = 0x(4n+3)e - (i2\pi(4n+3)kN)DFTN\\ 2[x(2n)] + WkNDFTN4(x(4n+1)) + W3kNDFTN4(x(4n+3)) \end{split}$$

3. BUTTERFLY UNIT

The butterfly unit is designed to perform to compute radix-4 or radix-2 DIF FFT algorithm, it has the pipeline structure with total 4 pipeline stages. The rst, second and third pipeline stages perfor itccan perform radix 8 .when it is diffuct to calculate radix 8 operation with the help of butterfly unit it perform in the form of radix 2 and radix 4.

4. TWIDDLE-FACTOR GENERATOR

recursive feedback difference equation for the computation of sine and cosine functions. We use the recursive sine/cosine function generator. This method has the advantage of low complexity progress

there are two parts of input i.e real-xinr anr imagenary xinn



Fig. 3. The structure of proposed FFT processor.

REFERENCES

- [1] P. L. Montgomery, "Modular multiplication without trial division," Math.
- [2] Comput., vol. 44, no. 170, pp. 519–521, Apr. 1985.
- [3] C. McIvor, M. McLoone, and J. V. McCanny, "Modified Montgomery
- [4] modular multiplication and RSA exponentiation techniques,"
- [5] Proc.-Comput. Digit. Techniques, vol. 151, no. 6, pp. 402–408, Nov. 2004.
- [6] S.-H. Wang, W.-C. Lin, J.-H. Ye, and M.-Shieh,
- [7] Montgomery Modular Multiplier," in Proc. IEEE International
- [8] Symposium on Circuits and Systems, May 2012, pp. 3049–3052.
- [9] S. C. Lai, W. H. Juang, C. C. Lin, C. H. Luo, and S. F. Lei, "High-Throughput, Power-Efficient, Coefficient-Free and Reconfigurable Green Design for Recursive DFT in a Portable DRM Receiver," International Journal of Electrical Engineering, vol. 18, no.3, pp. 137–145, June 2011
- [10] S. C. Lai, S. F. Lei, C. L. Chang, C. C. Lin, and C. H. Luo, "Low Computational Complexity, Low Power, and Low Area Design for the Implementation of Recursive DFT and IDFT Algorithms", IEEE Trans. CircuitsSyst. II, Exp. Briefs, vol. 56, no. 12, pp. 921-925, Dec. 2009



- [11] Ansuman DiptiSankar Das, Abhishek Mankar, N Prasad, K. K. Mahapatra, and Ayas Kanta Swain, "Efficient VLSI Architectures of Split-Radix FFT using New Distributed Arithmetic", International Journal of Soft Computing and Engineering (IJSCE), vol. no. 3, issue 1, pp. 264 -271, Mar. 2013.
- [12] S Compact RDFT Processor for the Computations of DFT and IMDCT in a DRM and DRM+ Receiver," J. Low Power Electron. Appl., vol. 3, no. 2, pp. 99-113, May 2013.