A Parallel Input Series Output DC/DC Converter with High Voltage Gain

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Abstract - The importance of high voltage gain dc/dc converter is increasing day by day. Conventional boost converter is unable to provide high gain without extreme duty ratio. An input parallel output series boost converter can provide a high step up gain. The converter uses two switches, two coupled inductors and a voltage multiplier module. The primary windings of coupled inductors are placed across the supply. Their connection reduces the input current ripple as it is shared by windings. The converter has high voltage gain and low voltage stress across power switches. The switches are turned on at zero current due to the leakage inductance of coupled inductor. The simulation of the converter is done in MATLAB/SIMULINK and results are obtained.

Key Words: High step up gain, DC/DC converter, Low voltage stress, Coupled inductors.

1. INTRODUCTION

High gain dc/dc converters are widely used in many industrial applications such as solar, fuel cell, x-rays, laser and high intensity discharge lamp ballasts for automobile headlamps[2]-[4]. Theoretically, a basic boost converter is capable of providing high conversion ratio, but extremely high duty ratio is required. In practice, extreme duty ratios are not permitted because of the large conduction losses and frequent damage of power switches. Usually it is preferable to use low voltage rated power switches having low on state resistance to reduce the conduction losses, which may not be possible in a conventional boost converter. Cascaded boost converters can provide high voltage gain[5]-[6]. But high voltage stress across the switches and poor efficiency are the disadvantages. DC/DC converters using coupled inductors is a good alternative to obtain a high step up gain[7], provided the leakage inductances are handled properly. Interleaved control is found very useful in reducing the input current ripple of the converter[8]-[10]. Two different boost converter structures can be combined to produce twice the voltage gain by connecting them in parallel and output in series. The two independent inductors of this combined converter is replaced by two coupled inductors. Connecting the primary windings of coupled inductors in parallel and secondary windings in series a high step up DC/DC converter is derived. An input parallel output series boost converter with dual coupled inductors can be used for high step up and high power applications. The interleaved control employed reduces the input current ripple considerably. This configuration inherits the merits of high voltage gain, low voltage stress across the power switches and low output voltage ripple. Also, the converter is capable to turn on the active switches at zero current and hence reduce switching losses.

2. PARALLEL INPUT SERIES OUTPUT DC/DC CONVERTER

2.1 Input parallel output series boost converter

The input parallel output series concept is explained in Fig 1 to 3. The basic boost converter topology is shown in Fig 1 and Fig 2 is another boost version with the same function in which the output diode is placed on the negative dc rail. Fig 3 is called a modified interleaved boost converter, which is an input-parallel and output-series configuration derived from two basic boost types. The derived converter has twice the voltage gain of a conventional boost converter, low output voltage ripple and low input current ripple due to interleaved control.
The separate inductors of Fig. 3 are modified by coupled inductors whose primary windings are connected in parallel and secondary windings in series as shown in Fig. 4. A voltage multiplier module is connected in the output to get a higher voltage gain. This connection has several advantages compared to conventional interleaved boost converter.

2.2 Operation of the converter

The converter is operated in continuous conduction mode (CCM). 180° interleaved overlapped pulses (Duty ratio greater than 50%) are used for the power switches. There are three switching states as S1: ON, S2: ON; S1: ON, S2: OFF; S1: OFF, S2: ON. Operation of the converter can be explained through eight modes in the above mentioned control scheme. The basic working principle is as explained below. The theoretical waveforms of the converter are shown in Fig. 5. The schematic diagram in each operating mode is shown in Fig. 6 to Fig. 13.

Mode 1[t0-t1]: At t=t0 Switch S1 is turned on at zero current switching due to the leakage inductance of Lk1. S2 remains turned on from the previous state as shown in Fig. 6. All diodes except output diode D3 is turned off. This phase ends when the current through D3 decreases to zero.

Mode 2[t1-t2]: In this stage the power switches S1 and S2 remains turned on, as shown in Fig. 7. All of the diodes are
reversed-biased. The voltage source \( V_{in} \) charges magnetizing inductances \( L_{m1} \) and \( L_{m2} \) as well as leakage inductances \( L_{k1} \) and \( L_{k2} \). This stage ends at \( t_2 \) when \( S_2 \) is turned off.

**Fig -7: Mode 2**

**Mode 3\([t_2-t_3]\):** The switch \( S_2 \) is turned off at \( t = t_2 \), hence the diodes \( D_2 \) and \( D_r \) turned on. The current flow direction is shown in Fig -8. The energy that has stored in magnetizing inductance \( L_{m2} \) is transferred to the secondary side, charging the capacitor \( C_r \) through \( D_r \). The input voltage source \( V_{in} \), magnetizing inductance \( L_{m2} \) and leakage inductance \( L_{k2} \) deliver energy to the capacitor \( C_2 \) through diode \( D_2 \).

**Fig -8: Mode3**

**Mode 4\([t_3-t_4]\):** when the total energy of leakage inductance \( L_{k2} \) has been completely delivered to the capacitor \( C_2 \) at \( t = t_3 \), diode \( D_2 \) automatically switches off. The current flow path of this stage is shown in Fig -8. Magnetizing inductance \( L_{m2} \) will transfer energy to the secondary side charging the capacitor \( C_r \) through diode \( D_r \). The sum of currents of the magnetizing inductances \( L_{m1} \) and \( L_{m2} \) flows through the switch \( S_1 \).

**Fig -9: Mode 4**

**Mode 5\([t_4-t_5]\):** The switch \( S_1 \) remains turned on at \( t = t_4 \), the switch \( S_2 \) is turned on with ZCS due to the leakage inductance \( L_{k2} \). The current flow direction of this stage is shown in Fig -10. This stage ends when the current through the diode \( D_r \) reduces to zero at \( t = t_5 \).

**Fig -10: Mode 5**

**Mode 6\([t_5-t_6]\):** Operating modes 2 and 6 are same. All diodes are turned off. The magnetizing inductances \( L_{m1} \), \( L_{m2} \) and the leakage inductances \( L_{k1} \), \( L_{k2} \) are charged by the source.

**Fig -11: Mode 6**

**Mode 7\([t_6-t_7]\):** The switch \( S_2 \) remains turned on. Switch \( S_1 \) gets turned off at \( t = t_6 \). Which bring \( D_1 \) and \( D_3 \) into
conduction. The current flow path of this stage is shown in Fig-12. The source $V_{\text{in}}$, $L_{m1}$ and $L_{k1}$ together release their energy to the capacitor $C_1$ through the switch $S_2$. At the same time, the energy stored in $L_{m1}$ is released to the secondary side. $D_3$ is conducting and the current through the secondary sides will flow to load and capacitor $C_3$. 

![Fig-12: Mode 7](image)

Mode 8[$t_7$-$t_8$]: At time $t = t_7$, diode $D_3$ gets turned off because the total energy of leakage inductance $L_{k1}$ has been completely transferred to the capacitor $C_1$. The current of the magnetizing inductance $L_{m1}$ continues to flow to the output through the secondary side of coupled inductor and $D_4$ until $t_8$.

![Fig-13: Mode 8](image)

\[
m_{\text{CCM}} = \frac{2(kN+1)}{1-D} \tag{1}
\]

Where $k$ is the leakage factor of coupled inductors, $N$ is the turns ratio and $D$ is the duty ratio.

### 3.2 Voltage stress analysis

To simplify the voltage stress analyses of the components, the leakage inductance of coupled inductor and the voltage ripples on the capacitors are ignored. The voltage stresses on power switches $S_1$ and $S_2$ for an output voltage $V_0$ are derived as, [1]

\[
V_{S1} = V_{S2} = \frac{V_0}{2(1+N)} \tag{2}
\]

### 3.3 Coupled inductor design

From the voltage gain equation, the turns ratio of coupled inductor can be designed as, [1]

\[
N = \frac{m_{\text{CCM}}(1-D)}{2k} - \frac{1}{k} \tag{3}
\]

### 3.4 Capacitor design

The filter capacitors are designed considering the voltage ripple($\Delta V_C$) across it, for switching frequency $f_s$ and load resistance $R$ the capacitor values are estimated according to below equations [1]

\[
C_1 \geq \frac{D V_0}{\Delta V_C R f_s} \tag{4}
\]

\[
C_2 \geq \frac{D V_0}{\Delta V_{C2} R f_s} \tag{5}
\]

\[
C_3 \geq \frac{D V_0}{\Delta V_{C3} R f_s} \tag{6}
\]

\[
C_r \geq \frac{V_0}{\Delta V_{C2} R f_s} \tag{7}
\]

### 2. SIMULATION AND RESULTS

The converter is simulated in MATLAB/simulink and simulation results are obtained. The simulink model of the converter is shown in Fig-14. The pulse generation circuit is shown as a subsystem. 180° interleaved overlapped pulses are used. The control signals with duty ratio 0.5 are shown in Fig-15. The simulation parameters are shown in table 1.

### 3. CIRCUIT ANALYSIS AND DESIGN

#### 3.1 Voltage gain expression

Take two identical coupled inductors. Using the volt-second balance principle on magnetizing inductances $L_{m1}$ and $L_{m2}$ respectively, the voltage gain ($m_{\text{CCM}}$) can be obtained as, [1]
Fig -14: Simulink model IPOS high gain converter

Fig -15: Control pulses of switches

Table -1: Simulation parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P_o)</td>
<td>100W</td>
</tr>
<tr>
<td>(V_{in})</td>
<td>20</td>
</tr>
<tr>
<td>Magnetizing inductance, (L_{m1}, L_{m2})</td>
<td>242 (\mu) H</td>
</tr>
<tr>
<td>Capacitors (C_1, C_2)</td>
<td>47 (\mu) F</td>
</tr>
<tr>
<td>Capacitor (C_3)</td>
<td>100 (\mu) F</td>
</tr>
<tr>
<td>Capacitor (C_1)</td>
<td>10 (\mu) F</td>
</tr>
<tr>
<td>Switching frequency, (f_s)</td>
<td>40kHz</td>
</tr>
<tr>
<td>(V_{out})</td>
<td>200</td>
</tr>
</tbody>
</table>

Fig -16, 17 respectively shows the voltage across and current flowing through the switches 1 and 2. The voltage stress across the switch is a quarter of the output and switches are turned on at zero current.

Fig -18: Output voltage waveform

Fig -19: Voltage stress across diodes

Fig -20: Current through diodes

It is clear from the waveforms that the switches are turned on with zero current turn on due to the leakage inductance present in the path and hence switching losses are reduced.
Fig -21: Ripple comparison
The output voltage with an input of 20V shown in Fig - 18 proves that the converter achieves the expected voltage gain with a low duty ratio of 0.6. Fig -19 and Fig -20 respectively show the voltage across and current flowing through the diodes. Ripple comparison shown in Fig -21 proves that the converter has a very less input current ripple compared to conventional boost/interleaved boost converter.

3. CONCLUSIONS

An parallel input series output DC/DC converter using dual coupled inductors is found to be a good candidate for low input voltage, high voltage gain applications. The converter can achieve a much higher voltage gain and avoid operating at extreme duty cycle and numerous turn’s ratios. A voltage gain of 10 is obtained by operating at a duty ratio of 0.6 with turns ratio 1. The voltage stresses of the power switches are very low, which is 25% of the output voltage. Interleaved control reduces the input current ripple effectively. The output voltage ripple is calculated as 0.02%. The simulation results show that main switches can be turned on at zero current.

REFERENCES