

Quantitative Modeling and Simulation of Single-Electron Transistor

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Abstract— The Single electron transistor (SET) is a new nano scaled switching device that retains their scalability even on an atomic scale, which can offer ultra-low power consumption and high operating speed.

SET has some attractive feature like unique coulomb blockade oscillation characteristic, and nano-scale size. It is seen that energy quantization mainly increases the Coulomb blockade area and Coulomb blockade oscillation periodicity, and thus, affects the SET circuit performance. The transfer of charge onto the island becomes quantized as the voltage increase, leading to the current, so-called coulomb staircase. For it two conditions are required mainly, in first condition the electron thermal fluctuations energy smaller than the coulomb energy and in second condition, the tunnel effect itself should be weak enough to prevent the charge of the tunneling electrons from becoming delocalized over the two electrodes of the junctions.

The goal of this paper is to discuss about the DC characteristics of SET and the effect on characteristics of SET by variation of various physical parameters, is analyzed by MATLAB Simulink.

Key Words—Quantum tunneling, Coulomb blockade (CB), quantum dot (QD), energy quantization, single electron transistor (SET).

1. INTRODUCTION

Our world is without doubt built on the power of the transistor, a microscopic electronic switch used to perform digital logic. Right now, we are able to fit enough of these tiny devices onto a microchip to allow us to perform several billion operations in a single second, and are seeing a double in the speed of these microchips every 18 months. In order to keep up with this incredible rate of speed increase, transistors are becoming smaller and smaller, to the point where in the very near future, they will begin to not only feel the effects of quantum mechanics on their operation, but will have to take quantum mechanics into account as the dominant force in their engineering.

Most transistors today are MOSFETs, where a semiconductor source and drain of one doping type are separated by an oppositely doped bulk semiconductor. The bulk semiconductor is then separated by a layer of oxide from a gate electrode between the source and the drain. As the gate bias is changed, the bias causes the formation of a conducting channel in the bulk material between the

source and drain, allowing current to flow and thus turning the switch on. In a single electron transistor, however, charge moves by utilizing the effect of quantum tunneling. Instead of creating a channel of charge carriers between the source and drain electrodes, a single electron transistor utilizes two junctions where tunneling is the dominant method of electron transport to control the movement of single electrons through the device.

2. BASIC THEORY

2.1 QUANTUM TUNNELING

A single electron transistor is based on the idea of quantum tunneling.

In classical physics, when an electron is in a potential, it is unable to go anywhere, where the potential is higher than the energy of the electron fig.1.

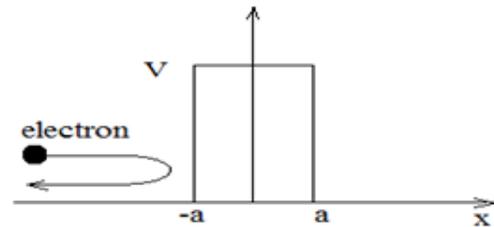


Fig. 1: Classical theory of electron Tunneling

However, According to the laws of quantum mechanics, when the size of the barrier is very small, the wave properties of the electron become relevant. And there is a non vanishing (larger than zero) probability for an electron on one side of the barrier to reach the other side.

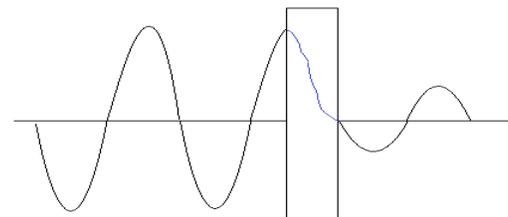


Fig. 2: quantum tunneling of electron

2.2 COULOMB BLOCKADE

In physics, a Coulomb blockade (abbreviated CB), named after Charles-Augustin de Coulomb's electrical force, is the increased resistance at small bias voltages of an electronic

device comprising at least one low-capacitance tunnel junction. Because of the CB, the resistances of devices are not constant at low bias voltages, but increase to infinity for zero bias (i.e. no current flows).

Due to the discreteness of electrical charge, current through a tunnel junction is a series of events in which exactly one electron passes (tunnels) through the tunnel barrier. The tunnel junction capacitor is charged with one elementary charge by the tunneling electron, causing a voltage buildup $V = \frac{e}{C}$ where e is the elementary charge of 1.6×10^{-19} coulomb and C the capacitance of the junction. If the capacitance is very small, the voltage buildup can be large enough to prevent another electron from tunneling. The electrical current is then suppressed at low bias voltages and the resistance of the device is no longer constant. The increase of the differential resistance around zero bias is called the Coulomb blockade.

2.3 CONDITION FOR COULOMB BLOCKED

To achieve the Coulomb blockade, three criteria have to be met:

The bias voltage must be lower than the elementary charge divided by the self capacitance of the island:

$$V < \frac{e}{C} \tag{1}$$

The thermal energy in the source contact and the thermal energy in the island must be below the charging energy or else the electron will be able to pass the QD via thermal excitation

$$k_B T < \frac{e^2}{C} \tag{2}$$

The tunnelling resistance R_t , should be greater than h/e^2 which is derived from Heisenberg's uncertainty principle.

$$R_t \gg \frac{h}{2\pi e^2} \tag{3}$$

$$R_t \gg 25813\Omega$$

$$\approx 26 \text{ k}\Omega$$

The Coulomb energy is given by

$$E = \frac{e^2}{2C_\Sigma} \tag{4}$$

Where e is the charge on an electron and C_Σ is the total capacitance of the source and drain junctions and the gate capacitor.

2.4 SINGLE ELECTRON TRANSISTOR

The simplest device, in which the effect of coulomb blockade can be observed, is the so-called single electron transistor.

It consists of two electrodes known as the drain and the source, connected through tunnel junctions to one common electrode with a low self- capacitance known as

the island. The electrical potential of the island can be tuned by a third electrode, known as the gate, capacitive coupled to the island, As shown in fig.3

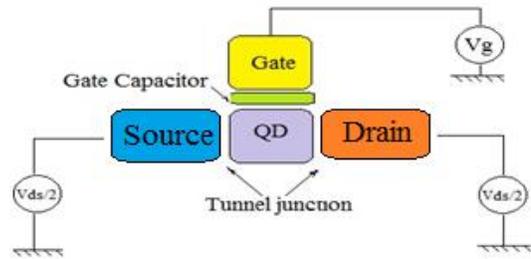


Fig. 3: Single electron transistor

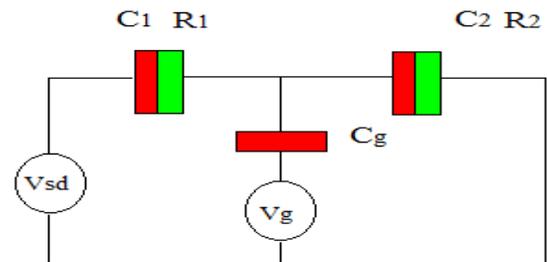


Fig. 4: capacitance model for the SET

3. MODELING AND SIMULATION METHODOLOGY

The Modeling and simulation of Single Electron Transistor is done using MATLAB Simulink. The SET circuit consisting of a dot between the source and drain electrodes separated by tunnel capacitors c_1 and c_2 . Both tunnel capacitors c_1 and c_2 have tunnel resistances R_1 and R_2 , respectively. The dot is also coupled to the gate electrode with capacitor C_g in order to control the current flow. The total capacitance between the dot and the outer environment can be written as C_Σ , where

$$C_\Sigma = C_1 + C_2 + C_g \tag{5}$$

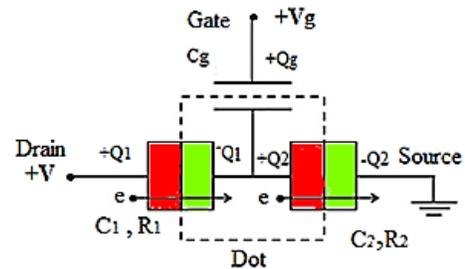


Fig. 5: Equivalent circuit of SET

There are four main equations for current-voltage characteristics of single electron circuits, i.e., free energy change ΔF , tunneling probability/rate Γ , steady state master equation and current equation I as follows.

3.1 Free energy change:

$$\Delta F_1^\pm(n_1, n_2) = \frac{e}{C_\Sigma} \left[\frac{e}{2} \pm (Ne - Q_0) \mp (C_g + C_2)V \pm C_g V_g \right] \quad (6)$$

$$\Delta F_2^\pm(n_1, n_2) = \frac{e}{C_\Sigma} \left[\frac{e}{2} \pm (Ne - Q_0) \mp C_1 V \pm C_g V_g \right] \quad (7)$$

Equations (6) and (7) are used to calculate the free (electrostatic) energy change ΔF of the system due to the one electron tunneling event. It is important to be noted that only tunneling events decreasing the electrostatic energy (and dissipating the difference) are possible.

3.2 Tunneling probability/rate:

The most important requirement for occurrence of single electron tunneling is that the total energy of the system must Decrease due to one electron tunneling. Electron tunneling rate in tunnel junction (Γ) can be calculated from derivation of Fermi Golden Rule.

$$\Gamma_1^\pm(N) = \frac{1}{R_1 e^2} \left[\frac{\Delta F_1^\pm}{1 - \exp\left(\frac{\Delta F_1^\pm}{k_b T}\right)} \right] \quad (8)$$

$$\Gamma_2^\pm(N) = \frac{1}{R_2 e^2} \left[\frac{\Delta F_2^\pm}{1 - \exp\left(\frac{\Delta F_2^\pm}{k_b T}\right)} \right] \quad (9)$$

The values ΔF from equations (6) and (7) are used to calculate electron tunneling probability in the equations (8) and (9), respectively. The tunneling of a single electron through a particular tunnel junction is always a random event, with a certain rate Γ (i.e., probability per unit time) which depends solely on the ΔF .

3.3 Steady State Master equation:

$$p(N) [\Gamma_2^-(N) + \Gamma_1^+(N)] = p(N+1) [\Gamma_2^-(N+1) + \Gamma_1^+(N+1)] \quad (10)$$

$$I(V) = e \sum_{N=-\infty}^{\infty} p(N) [\Gamma_1^+(N) - \Gamma_1^-(N)] \quad (11)$$

$$= e \sum_{N=-\infty}^{\infty} p(N) [\Gamma_2^+(N) - \Gamma_2^-(N)] \quad (12)$$

Equation (10) expresses the Master equation in steady state, resulting the value of $p(N)$, which is necessary to be used for the current calculation in equation (11) and (12). where e is the elemental charge, k_b is the Boltzmann constant, T is the temperature, N is the number of electrons in the dot, n_1 and n_2 are a number of electrons flows through the capacitor C_1 and capacitor C_2 , respectively, Q_0 is the background charge and \pm express that the electron tunnels through the capacitor with the direction from left to the right and from right to the left, respectively.

The iterative algorithm of master equation method is presented in Figure

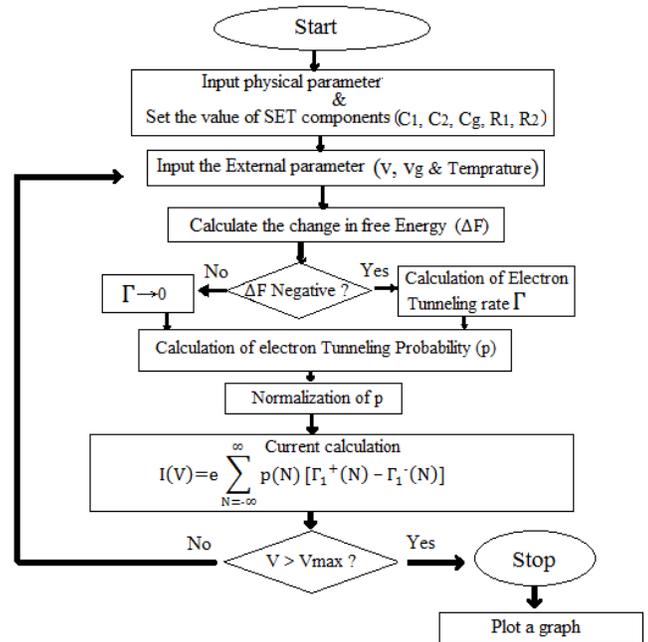
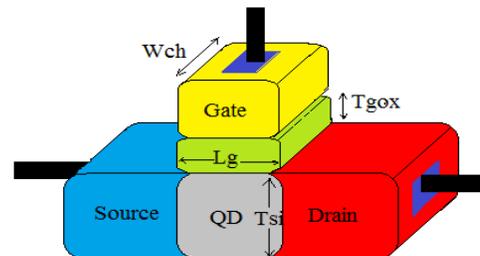


Fig. 6: algorithm of master equation

4. FABRICATION PARAMETERS:



The main fabrication parameters are source and drain tunnel junction capacitances, side gate capacitance, and control gate capacitance, are given below

$$C_g = \epsilon_{SiO_2} \left[\frac{Lg \times Wch}{T_{gox}} \right] \quad (13)$$

Where C_g , L_g , W_{ch} and T_{gox} are side gate capacitance, side gate length, channel width, and side gate oxide thickness respectively.

$$C_c = \epsilon_{SiO_2} \left[\frac{Lc \times Wch}{T_{cox}} \right] \quad (14)$$

Where C_c , L_c , & T_{cox} are control gate capacitance, control gate length and control gate oxide thickness respectively. Before any electron tunneling, the tunneling junctions act as capacitances so it could be written as:

$$C_1 = C_2 = \epsilon_{Si} \left[\frac{T_{si} \times Wch}{L_g} \right] \quad (15)$$

Where C_1 , C_2 , and T_{si} are source capacitance, drain capacitance, and channel thickness, respectively. But here in this paper I only assume that SET is three terminal

devices and neglect to Cc capacitance effect.

Some external parameters (V , V_g , T and q_0) and some device parameters (C_1 , C_2 , C_g , R_1 and R_2), effects the properties of the SET but there is difference between them parameter like device parameter may be set before fabrication and external parameter may be adjust according to environmental condition given in below table 1 [9]

Description	Value
Wch	15nm
Lg	20nm
Lc	10nm
Tgox	10nm
Tcox	5nm
Tsi	15nm

Table 1

Represents the approximate values of the parameters that is used for the fabrication of the silicon-based dual-gate SET [9].

5. RESULT AND DISCUSSION

The modeling of single electron transistor is based on its stability criteria for selecting parameters in such a way that all the characteristic of SET comes within the stability region, so below there is a brief discussion on stability and curve based on master's equation of SET.

5.1 Stability plot for SET:

The energy which determines electron transportation through a single-electron device is Helmholtz free energy which is defined as difference between total energy stored in the device and the work done by power source. Total energy stored includes all of energy components when an island is charged with an electron. For a SET with source and control gate terminals grounded, and drain and side gate terminals based at V_{ds} and V_{gs} , the free energy has been formulated as following.

$$F = E - Q_d \times V_{ds} - Q_g \times V_{gs} \quad (16)$$

Here E is the electrostatic energy, Q_g is the charge of the side gate capacitance, and Q_d is the charge at drain tunnel junction capacitance. The change of Helmholtz free energy is calculated as:

$$\Delta F = F_i - F_f \quad (17)$$

Where F_i and F_f are the Helmholtz free energy of the system before and after an electron tunneling happens respectively.

A tunneling could only happen if ΔF is negative. For a logic operation, i.e., where the number of electrons in the island is 0 or 1, ΔF is defined as:

$$\Delta F = V_{ds} \left(\frac{C_1}{C_\Sigma} \right) + V_{gs} \left(\frac{C_g}{C_\Sigma} \right) < 0 \quad (18)$$

For the electron tunneling of the island to the source terminal ΔF is:

$$\Delta F = -V_{ds} \left(\frac{C_1}{C_\Sigma} \right) - V_{gs} \left(\frac{C_g}{C_\Sigma} \right) < 0 \quad (19)$$

If an electron tunnels from the island to the drain terminal, ΔF is defined as:

$$\Delta F = V_{ds} \left(\frac{C_g + C_2}{C_\Sigma} \right) - V_{gs} \left(\frac{C_g}{C_\Sigma} \right) < 0 \quad (20)$$

For the electron tunneling of the drain terminal to the island, ΔF is:

$$\Delta F = V_{ds} \left(\frac{C_g + C_2}{C_\Sigma} \right) - V_{gs} \left(\frac{C_g}{C_\Sigma} \right) < 0 \quad (21)$$

The above equation (18-21) obtained from the equation 6 & 7.

Now in SET, V_{ds} versus V_{gs} characteristic is known as stability plot. This plot is obtained by setting equations (18-21) equals to zero. Thus four lines' equation will be obtained so that their cross creates a rhombus as shown below.

Slop of these lines has been formulated as following:

If electron tunnels from the island to the drain terminal and vice versa, lines' slope is:

$$S1 = \left[\frac{C_g + C_2}{C_\Sigma} \right] \quad (22)$$

If electron tunnels from the source terminal to the island and vice versa, lines' slope is:

$$S2 = \left[\frac{-C_g}{C_\Sigma} \right] \quad (23)$$

The stability plot of SET is illustrate in fig. (7)

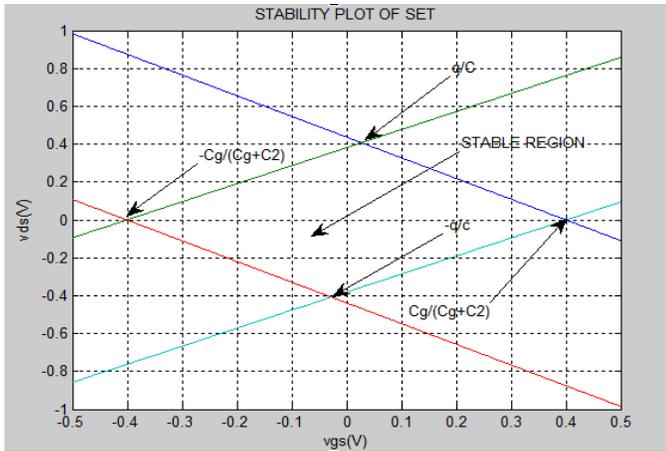


Fig.7. stability plot of SET for n=0

In this Figure the rhombus outside regions corresponds to regions with an integer number of the excess electrons on the island.

In rhombus inside, there is no excess electron on the island (The Coulomb Blocked Region).

But if charge will be present in this island region then stability criteria may be effected significantly, the stability region will be shifted in the right or left direction depend on the charge on the island, $n = \dots -2, -1, 0, 1, 2 \dots$ as shown in figure 8. Here $n=1, 2$ represents number of electron in quantum dot, $n=0$ shows empty quantum dot and $n=-1, -2$ shows holes in quantum dot.

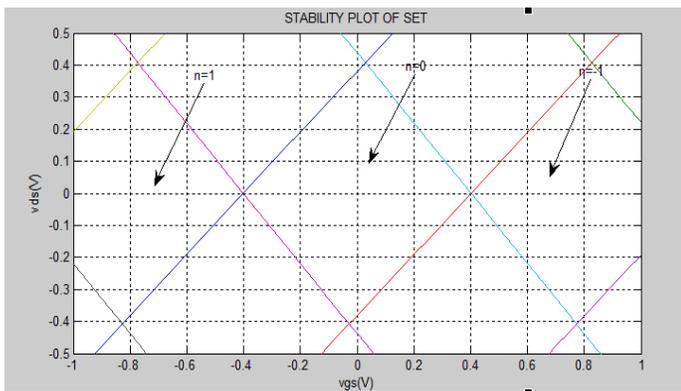


Fig. 8 shift in stability region

5.2 Current oscillation on variation in Vgs

For logic operation, if V_{gs} is increased and V_{ds} is kept constant below the Coulomb blocked, $|V_{ds}| < \frac{q}{C}$, the current will oscillate with the period of $\frac{q}{C_g}$ Figure (9). This is because of V_{ds} is not applied or increasing in accordance to pull the electron from source to QD to Drain for a continuous current. And thus V_{gs} is showing the control over transportation of electron from source to drain.

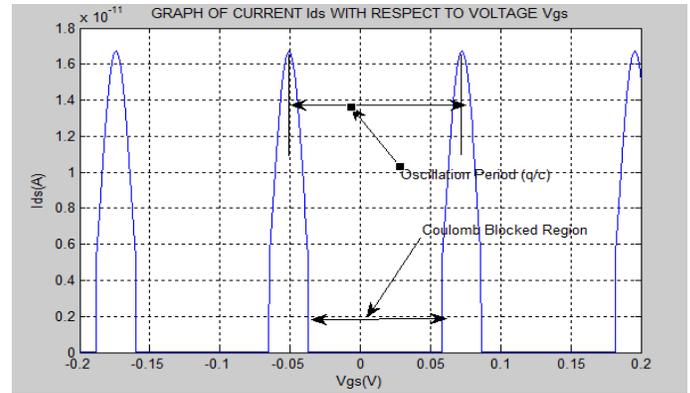


Fig. 9. current oscillation with logical operation on V_{gs}

Now to analysis the dc characteristic of SET, firstly it is assume that V_{ds} may be zero or may have any fixed value. From equation 13-15, It is shown in Fig.10 that, by increase of the channel width, the Coulomb blockade region becomes narrower and the oscillation period of the drain current decreases. This is because by increase of the channel width, all capacitances change but the slope of S_2 remains constant and the slope of S_1 reduces, so rhombus inside area or the Coulomb blocked region decreases. In addition, the side gate capacitance decrease, therefore the oscillation period of the drain current decreases.

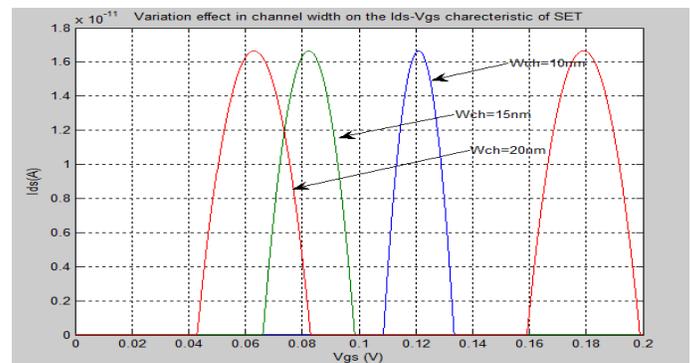


Fig 10: Variation effect in the channel width on the I_{ds} - V_{gs}

Fig.11 shows the side gate length variation effect on the I_{ds} - V_{gs} . It is demonstrated that, the increase of the side gate length causes the Coulomb blocked region to become narrower and the oscillation period of the drain current to become less. According to the equations (13-15), by increase of the side gate length, all capacitances are changed but the slope of S_2 remains constant and the slope of S_1 reduces, so the Coulomb blocked region decreases. The variation effect in the side gate length is less than the Variation effect in the channel width.

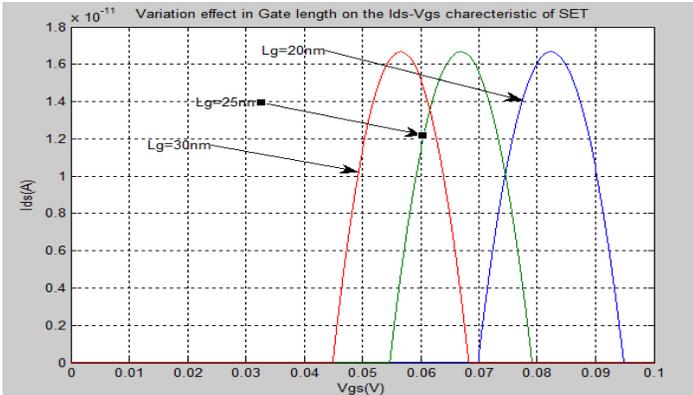


Fig 11: Variation effect in the gate length on the I_{ds} - V_{gs}

It is demonstrated that, by increase of the side gate oxide thickness, the Coulomb blocked region becomes wider and the oscillation period of the drain current increases. According to equation 13-15, increase of this parameter causes the side gate capacitance to become less and the slope of both $S1$ and $S2$ to increase. Shown in fig12

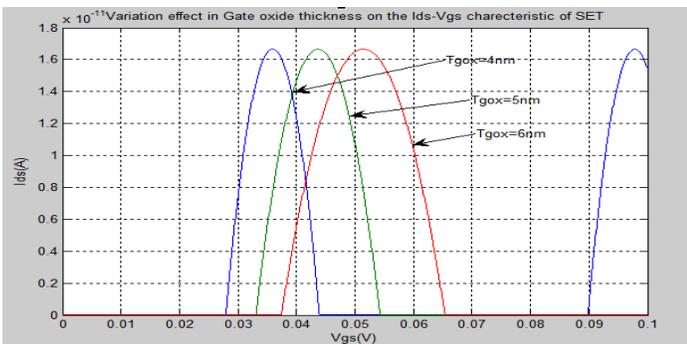


Fig12: Variation effect in the gate oxide thickness on the I_{ds} - V_{gs}

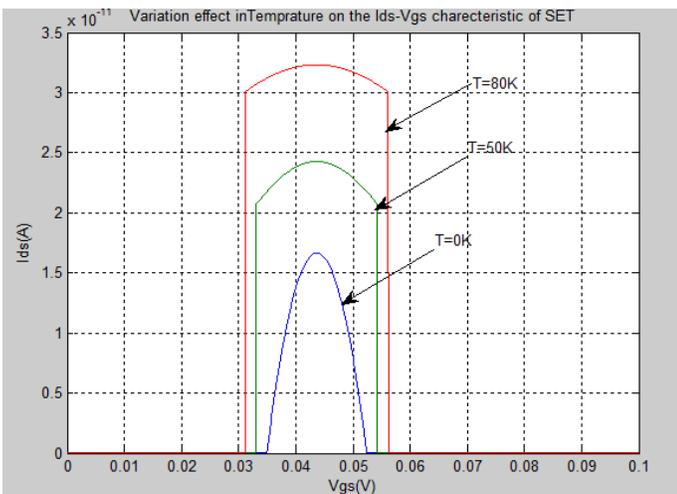


Fig 13: Variation effect in temperature on the I_{ds} - V_{gs}

Above fig 13 demonstrates the temperature variation effect on the I_{ds} - V_{gs} characteristic

5.3 Stair-Case I_{ds} current

For simulations purpose it is assumed that V_{ds} is varied from -1v to 1v, $T=20$ K and assume gate voltage $V_g=0$ in case of I_{ds} - V_{ds} characteristic and assume V_g varied from -0.2v to 0.2v, $V_{ds}=18$ mv and $T=2$ k . and from equation (11) and (12) we can plot I_{ds} - V_{ds} characteristic plot shows the device is symmetric.

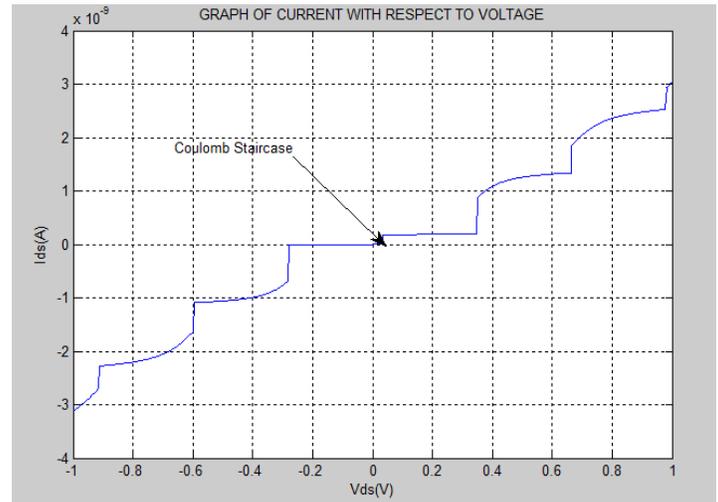


Fig.14. I-V characteristic plot.

As shown as the coulomb staircase effect in I_{ds} - V_{ds} characteristic the may be too much effected by temperature variation as shown in Fig.15

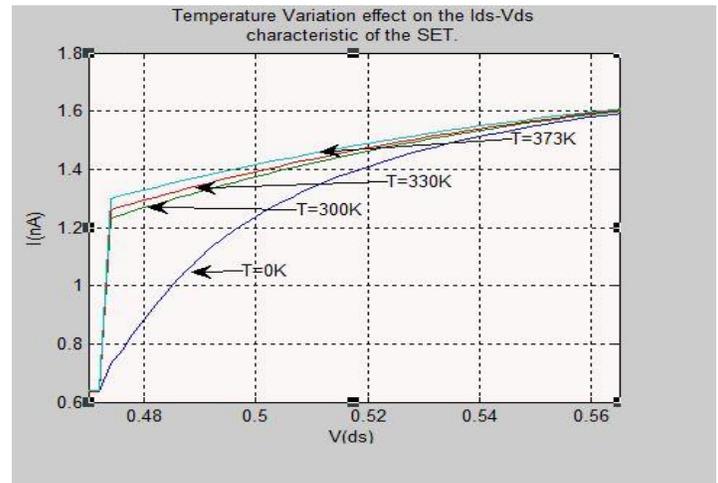


Fig15: temperature variation effect on the I_{ds} - V_{ds}

There is an increase in the value of current as temperature increases and there is also a very small difference in the value of the current when temperature becomes at high value range but there is all must reverse result will be obtained when increase in the value of background charges as shown in Fig.16

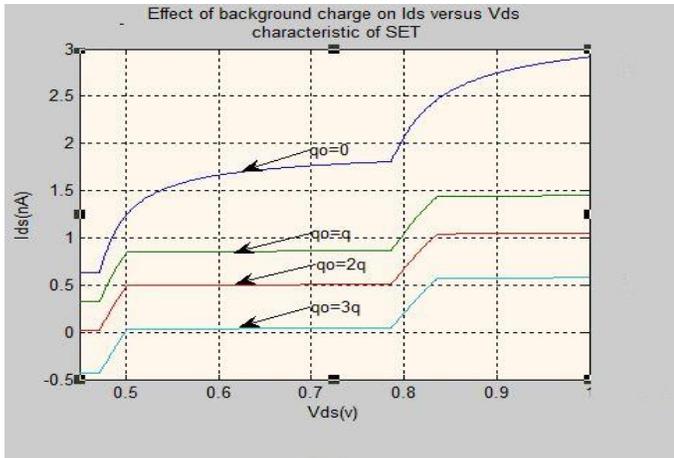


Fig 16: Background charge variation effect on the I_{ds} - V_{ds}

So this is good for SET I_{ds} - V_{ds} characteristic that there are no charges in the island.

6. CONCLUSION

In conclusion, I have demonstrated the electrical characteristic of SET by using Master Equation approach and show a fairly accurate result with experimental data. Evidently, staircase pattern of I-V characteristic are clearly obtained as the main role of coulomb blockade effect in the SET system.

This research paper focuses the theoretical discussion of basic principle of SET with importance of SET in the era of nanotechnology to provide low power consumption and high operating speed in the field of VLSI design for the fabrication of various electronic devices. SET has proved its value as tool in scientific research. The main problem in nanometer era is the fabrication of nano scale devices that can be achievable by the use of SET.

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8. BIOGRAPHIES



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