AN ULTRA LOW VOLTAGE, WIDEBAND LOW NOISE AMPLIFIER DESIGN TECHNIQUE

Aparna Singh Kushwah[1], Safalta Katare[2]

[1]*Asst. Professor, UIT, RGPV Bhopal*
[2] *M.E. Scholar, UIT, RGPV Bhopal*

Abstract - *Low noise amplifier (LNA) is a vital segment of RF receiver and frequently required to operate at wide frequency bands for various wireless system applications. For wideband operation, critical execution measurements, for example, power dissipation, s-parameter, noise figure and linearity have been carefully researched and described for the proposed LNA. This work introduces a low noise amplifier (LNA) utilizing current reuse system for wideband receiver. The current reuse strategy is routed to optimize noise performance and power efficiency while keeping up a decent power gain and input/output matching. An inductive peaking configuration is effectively utilized in the proposed LNA which incorporates cascaded networks with a peaking inductor in the buffer stage. Inductive peaking in the feedback loop is utilized to improve the bandwidth and noise performance of LNA.*

Key Words: **Current reuse, inductive series peaking, low- noise amplifier (LNA), ultra-low voltage (ULV), ultra-wideband (UWB)**.

1. INTRODUCTION

A Low Noise Amplifier which is the front end of the radio receiver plays an important role for the signal amplification in communication systems. A radio receiver gives the usable information to the users by converting the radio waves present in an environment. It has LNA, mixer and filter in which LNA plays the major role of amplification. The basic configuration of LNA comprises of RF amplifier in the middle of input matching and the output matching network. The demand of LNA increases due to the development of the modern technologies such as GPS, Bluetooth, cell phones etc. The LNA amplifies the weak signal received by the antenna in the receiving end. Mostly in wireless communication system the LNA is critical to design because it should provide enough gain from the low power signal which is received by the antenna, not only to make signal to noise ratio degradation but also to sustain signals with low power dissipation.

The rest of this paper is organized as follows. Section 2 manages the design challenges of LNA to accomplish maximum gain and minimum power consumption. Section 3 outlines the design of proposed circuit. Section 4 deals with the simulations and discussions. Section 5 deals with conclusions. Section 6 deals with the reference papers.

2. LNA DESIGN CHALLENGES

A LNA combines a low noise figure, reasonable gain, and stability without oscillation over entire useful frequency range. The LNA work, assume an essential part in the receiver design. Its fundamental capacity is to amplify extremely low signals without adding noise, saving the expected Signal-to-Noise Ratio (SNR) of the framework at to a great degree low power levels. Also, for large signal levels, the LNA enhances the received signal without introducing any distortions, which eliminates channel interference. LNA design should meet different challenges like good transistor selection, high gain, suitable DC biasing network, low noise figure, high linearity, good input-output matching circuits, and good stability.

Transistor determination is the first and most essential step in an LNA design. The transistor choice ought to be deliberately looked into, keeping the most vital LNA design trade-offs as a primary concern.

- An LNA configuration displays an impressive test due to its concurrent prerequisite for high gain, low noise figure, good input and output matching and unconditional stability at the most reduced conceivable current draw from the amplifier.
- Although Gain, Noise Figure, Stability, Linearity and input and output match are for the most part similarly essential, they are associated and don't generally work in each other's support.
- Low noise figure and good input match is to be simultaneously obtained
- Unconditional stability will dependably require a certain gain reduction because of either shunt or series resistive loading of the collector. High IP3 requires higher current draw, in spite of the fact that the most minimal conceivable noise figure is generally accomplished at lower current levels.
- Additional improvement of IP3 can likewise be accomplished by proper power output matching (1dB compression point match or P1dB match). The P1dB coordinate, being not quite the same as conjugate match, diminishes the gain albeit enhancing IP3 execution.

3. LNA CIRCUIT DESIGN

In this paper, the LNA design is started with the basic configuration followed by a broad band LNA design. The analysis of low noise amplifier is completed by analysis of S parameters, power dissipation and noise analysis. LT-Spice software is used which provides an integrated circuit design for wireless applications such as satellite communication, mobile phones, pagers, radar systems, wireless networks, and high-speed data links. LT-Spice supports every step of the design of proposed work; schematic capture, time-domain, frequency domain, circuit simulation, and electromagnetic field simulation and optimize an RF design without changing tools.

Transistor determination is the first and most essential advance in a LNA design. The transistor should fulfill every one of the design parameters at the most reduced conceivable current and lower power consumption while working with higher frequency. The transistor choice for the LNA additionally relies on the desired frequency range. Table-I shows the transistor specifications used in the proposed circuit. An LC circuit is used in the first section of the circuit based on Pole Zero Compensation Technique. It acts as a lead-lag network.

The proposed circuit uses current reuse technique. Current Reuse is a strategy used to lessen the power dissipation in low noise amplifier by utilizing the current generated by driver transistor will bias the load. The current-reuse topology may give the best blend of high power increase, low noise figure, and low power utilization, making it a practical contender for use in UWB LNA designs. In an amplifier utilizing current-reuse techniques, the input RF signal is amplified by two cascaded common-source amplifier stages to give high gain. In the meantime, this topology likewise underpins low noise figures. The current-reuse technique is outstanding for its utilization in LNAs, for its ability of accomplishing high performance with power consumption that is not as much as traditional two-stage common-source amplifiers

This paper presents inductive series peaking for transfer speed upgrade of low-voltage CMOS current-mode circuits. It helps the data transmission by using the reverberation qualities of LC systems. Lastly, Gain Flattening, also known as gain equalizing is utilized to level or smooth out unequal flag powers over a predetermined wavelength run.

The component specification is provided in the table below.

Component	Value
M1	Rds(on) = 0.0126 Qgate(C) = 2.6e-008
M2	Rds(on) = 0.033 Qgate(C) = 2.1e-008
M3	Rds(on) = 0.165 Qgate(C) = 8e-009
M4	Rds(on) = 0.0055 Qgate(C) = 2.32e-007
C1	100mF
C2, C3	100fF
C4	5F
Rf	10Ω
L1, L2	3.1fH
L3	200pH
L4	200µH
L5	10µH
L6	200pH

Table-I Component Specifications

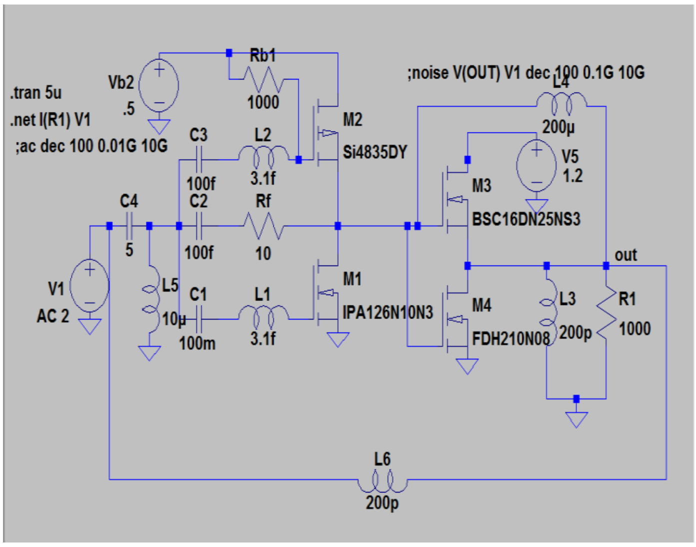

Fig -1: Complete schematic for proposed LNA

4. SIMULATION RESULTS

There are certain parameters which are very important in design and verification of Low Noise Amplifier. The parameters are stimulated and presented below.

4.1 S Parameter

Scattering parameters or S-parameters (the components of a dispersing grid or S-framework) portray the electrical conduct of straight electrical systems while experiencing different consistent state boosts by electrical signs. In this work, great input impedance matching was accomplished. Inductive peaking technique of the input helps in characterizing the matching bandwidth and the matching center frequency. The input return loss simulation results are shown in Fig.2 which demonstrate that S11 < -10 dB. This demonstrates the match of the proposed UWB LNA to the radio frequency signal receiving antenna

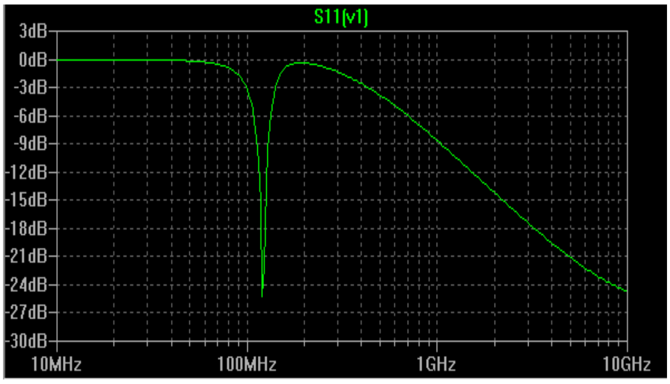

Fig -2: Simulation Results of S11

Fig.3 shows the simulation results of the output return loss. This great coordinating was accomplished with the assistance of peaking technique used. Also, the optimization of the second cascaded contributes in accomplishing this match state. Fig.3 represents the great match condition of the proposed low noise amplifier to its load.

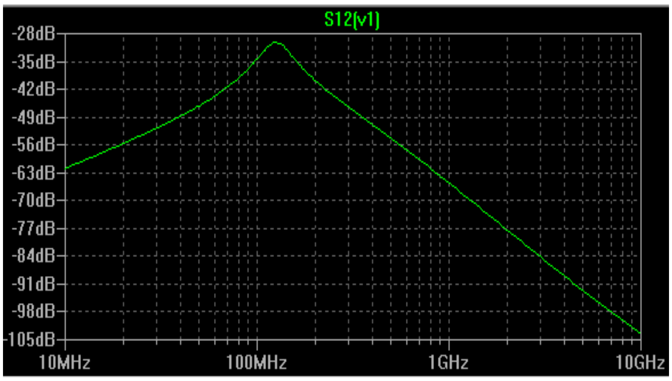

Fig -3: Simulation Results of S12

4.2 Power Dissipation

The power utilization is a genuine worry for the LNA. The LNA exhibited here accomplishes the low power utilization and utilizes low supply voltage. The power dissipation in the proposed LNA is in nW.

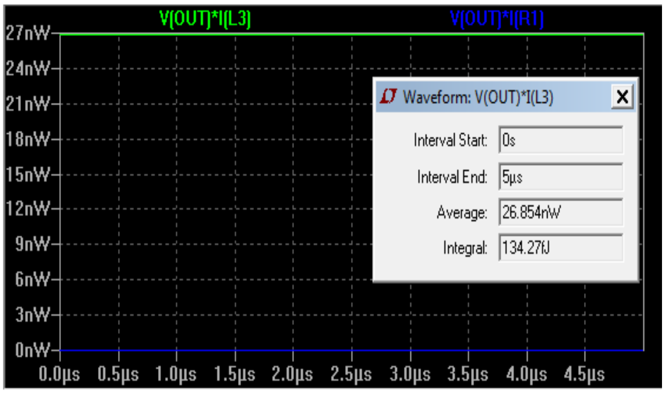

Fig - 4: Simulation Results of Power Dissipation

4.3 Noise

Noise figure is likewise one of the fundamental components for deciding the effectiveness of a LNA, subsequently can pick which LNA is reasonable for a specific application. The proposed LNA noise simulation results are shown in Figure 5.4. Low noise figure gives the outcome in improved reception of signal. LNA requires too small noise in the input device. The LNA configuration exhibited offers comparable performance in terms of gain, Noise Figure and linearity. The input noise is in nV while the output noise achieved with the proposed circuit is in µV.

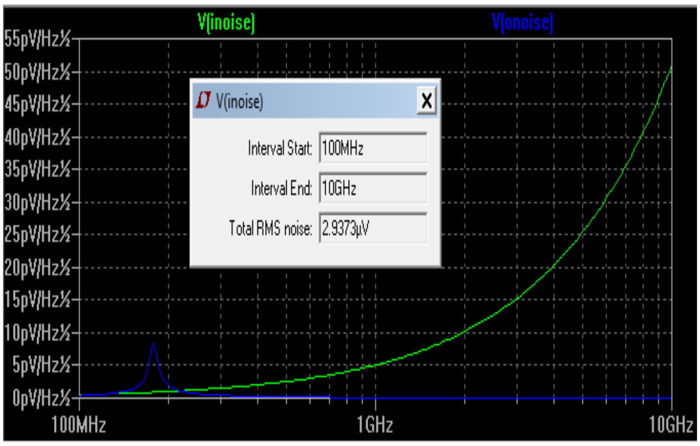

Fig -5: Simulation Results of Input Noise

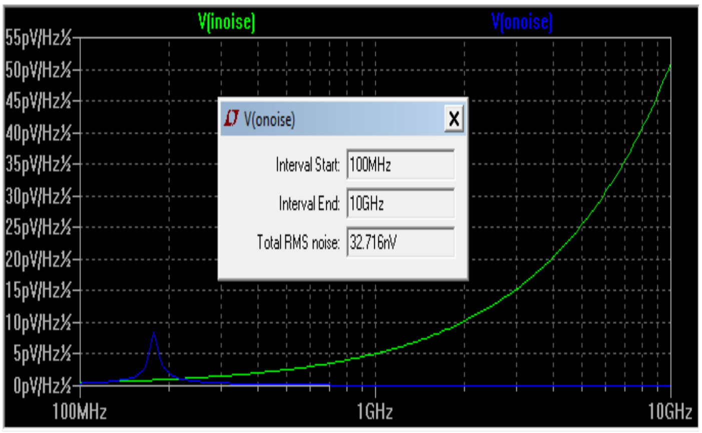

Fig -6: Simulation Results of Output Noise

5. CONCLUSIONS

The LNA is the main part of radio receiver. All design parameters reflects the quality of a Low Noise Amplifier. The LNA is designed to amplify the weak signal to provide the appropriate working condition to the mixer and to attenuate the noise level. In this paper, a ULP, ULV wideband CMOS LNA is proposed and intended for low-power and low voltage circuit plan. This paper highlights the design challenges. The work gives idea about the technique used to improve linearity of amplifier, technique to improve noise

International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 04 Issue: 11 | Nov -2017 www.irjet.net p-ISSN: 2395-0072

figure, reduce power consumption and provides good impedance matching in input and output section of amplifier A system simulation environment has been built using LT Spice software. It was found that the average power dissipation is 26.854Nw, S11< -10dB, input noise is in µV whereas output noise is in nV.

REFERENCES

[1] Pratap Kumar Dakua, Addala Satya Narayana Varma, P. Kabisatpathy: "Study on design and performance analysis of low noise high speed amplifier", 2016 International Conference on Signal Processing, Communication, Power and Embedded Systm (SCOPES)

[2] Madiha Hajri; Dalenda Ben Issa; Hekmet Samet: "Low noise amplifier for MB-OFDM UWB receivers", 2016 17th International Conference on Sciences and Techniques of Automatic Control and Computer Engineering (STA)

[3] Anish Kumar Verma; Sanjay Kumar: "Resistive Feedback Low Noise Amplifier for Software Defined Radio", 2016 Online International Conference on Green Engineering and Technologies (IC-GET)

[4] Maissa Daoud , Hassene Mnif , Mohamed Ghorbel, "A low power low noise amplifier for 2.45GHz ISM receiver for Body Area Network", 2016 11th International Design & Test Symposium (IDT)

[5] Vivek Singh, Munish Rattan, "Ultra wide band low noise amplifier with self-bias for improved gain and reduced power dissipation", International Conference on Computing, Communication and Automation (ICCCA)

[6] Amir Mahdavi; Fatemeh Geran : "A low power UWB CMOS low noise amplifier for 3.1–10.6 GHz in receivers", 8th International Symposium on Telecommunications (IST),2016

[7] Mahidi Parvizi, Karim Allidina, Mourad N. El-Gamal : "A Sub-Mw, Ultra-Low-Voltage, Wideband Low Noise Amplifier Design Technique", IEEE Transactions on Very Large Scale Integration, 2015

[8] A. Cagri Ulusoy : "A SiGe D-Band Low-Noise Amplifier Utilizing Gain Boosting Technique", IEEE, 2015

[9] Hardik Sathwara, Kehul Shah, "Design of low power CMOS low noise amplifier using current reuse technique", 5th Nirma University International Conference on Engineering (NUiCONE), 2015

[10] P. K. Verma, Priyanka Jain, "A low power high gain low noise amplifier for wireless applications"

[11] Paria Jamshidi, "An ultra wideband low-power low-noise amplifier using coupled inductors", 23rd Iranian Conference on Electrical Engineering, 2015