

# Netlist Optimization for CMOS Place and Route in MICROWIND

Mahesh G. Jaiswal<sup>1</sup>, Varsha Bendre<sup>2</sup>, Vinay Sharma<sup>3</sup>

<sup>1</sup>PG Scholar, Dept. of ME VLSI & Embedded, PCCOE Pune, Maharashtra, India

<sup>2</sup>Assistant Professor, Dept. of ME VLSI & Embedded, PCCOE Pune, Maharashtra, India

<sup>3</sup>Technical Director, Ni Logic Pvt. Ltd. Pune, Maharashtra, India

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**Abstract** - Microwind is a software tool which is used for CMOS IC layout design. The gate level design is created in schematic editor and simulator tool DSCH. The transistor size in the last few decades is shrinking drastically with the rapid advancement of VLSI technology to integrate more number of transistors on a single IC chip. This will indirectly affect the complexity in the placement and routing of the logic devices. And for any tool it is always a challenging task to make an efficient placement and routing of the cells. One of the EDA tool for CMOS design is MICROWIND, which uses a verilog net list generated by a schematic editor DSCH. This paper focuses on improvement in Microwind tool by implementing a logic optimization method for rearranging verilog net list according to interconnect wire nodes and number of logic cells like CMOS inverter, AND, OR etc. gates using MOS at 120nm technology and using FINFETs at 14nm technology. Our algorithm will rearrange net list and cells without reducing the actual transistors count. Therefore only the total numbers of metal layers, area of chip and interconnect delay etc. will get reduced to produce an optimum design.

**Key Words:** Area, DSCH, Frontend-Backend design, Logic Synthesis, MICROWIND, Net list, Optimize, Placement, Routing, etc.

## 1. INTRODUCTION

VLSI is the process of combining thousands of transistors into single Integrated Circuit (IC) chip. Interconnecting wires length increases with the increase in transistors in the circuit. It is difficult to reduce the capacitive and resistive effects which have an impact on time delay. The interconnecting wires also have fixed area and width making length as the only controllable parameter. Due to this there is a need of optimization techniques in VLSI design. In a Hardware Description Language like Verilog or VHDL, a net list is a description of all the devices or gates and all of the connections or wires between each device. In its simplest form, a net list consists of a list of the terminals (i.e. "pins") of the electronic components in a circuit and a list of the electrical conductors that interconnect the terminals. A net is a conductor that interconnects two or more component terminals. [6]

The objective of this paper is to develop an optimization logic that will automatically rearrange the verilog net list and create an efficient layout of the design in Microwind program. For the simulation purpose and observing the result of net list optimization logic, DSCH and MICROWIND

tool is required. The basic idea is to optimize the net list generated after successful design of any analog, digital or sequential circuit in schematic editor tool i.e. DSCH. According to that net list a layout is generated in MICROWIND tool which should be as much efficient to design a chip. This must be optimized in concern with area, interconnect, costing, metal routing etc.

To design an IC, VLSI IC design flow must be followed by the designer. The ASIC design flow is as shown in fig. 1. This design flow is mainly divided into two parts i.e. Frontend and Backend. This fig 1 shows few steps of the ASIC design. This paper introduces an optimization logic which must be applied in between Gate Level Net list and Floor planning step. A gate-level net list is a description of the circuit in terms of gates and connections between them, which are made in such a way that they meet the timing and power requirements. The actual placement of all logic cells is done in the way of gate level net list is arranged. Here in MICROWIND, a verilog net list decides the floor planning, placement of cells and their input-output routing.

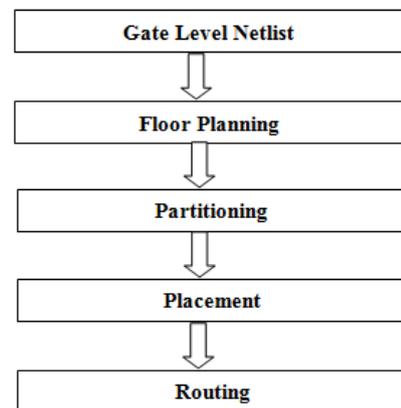


Fig 1: VLSI IC Design Flow

After compiling the verilog net list in MICROWIND, the floor planning, Partitioning, Placement and routing steps are done at the backend to produce a CMOS layout. Placement of cells and routing within the cells is becoming a difficult task for the designer as number of small sized transistors increases. To make this backend process as well as CMOS layout more efficient, optimization logic must be applied before the floor planning and placement steps. For physical layout structure and time optimization the various techniques like mapping, cell sizing, buffering and logic restructuring etc. can be

applied. This paper uses one of them i.e. logic restructuring technique.

## 2. TOOLS AND PLATFORM

### 2.1 MICROWIND

The MICROWIND software allows the designer to simulate and design an integrated circuit at physical description level. Born in Toulouse (France), MICROWIND is an innovative CMOS design tool for educational market. MICROWIND is developed as comprehensive package on windows platform to enable students to learn smart design methods and techniques with more practice. With inbuilt layout editing tools, mix-signal simulator, MOS characteristic viewer and more, it allows students to learn complete design process with ease. MICROWIND unifies schematic entry, pattern based simulator, SPICE extraction of schematic, Verilog extractor, layout compilation, on layout mix-signal circuit simulation, cross sectional & 3D viewer, net list extraction, BSIM4 tutorial on MOS devices and sign-off correlation to deliver unmatched design performance and productivity.

With its approach for CMOS design education, MICROWIND has gained lot followers worldwide. Universities across the globe are using MICROWIND for budding engineers to teach CMOS concepts with ease. Paving their path for more skilled software's to be used at later stage of their course work. [5]

### 2.2 DSCH

DSCH stands for Design Schematic Editor Tool. The DSCH program is logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user friendly environment for hierarchical logic design and fast simulation with delay analysis, which allows the design and validation of complex logic structures. DSCH also features the symbols, models and assembly support for 8051 & 16F84 controllers. Designers can create logic circuits for interfacing with these controllers and verify software programs using DSCH. [5]

### 2.3 PASCAL

Pascal is an imperative and procedural programming language, which is designed as a small, efficient language using structured programming and data structuring. A derivative known as Object Pascal designed for object-oriented programming. Pascal has introduced concepts and mechanisms which enabled programmers to define their own complex data types, and also made it easier to build dynamic and recursive data structures such as lists, trees and graphs. Important features included for this were records, enumerations, sub-ranges, dynamically allocated variables with associated pointers, and sets. To make this possible and meaningful, Pascal has a strong typing on all

objects, which means that one type of data cannot be converted or interpreted as another without explicit conversions [7]. We are using this scripting language as platform for implementation of the optimization logic.

## 3. METHODOLOGY

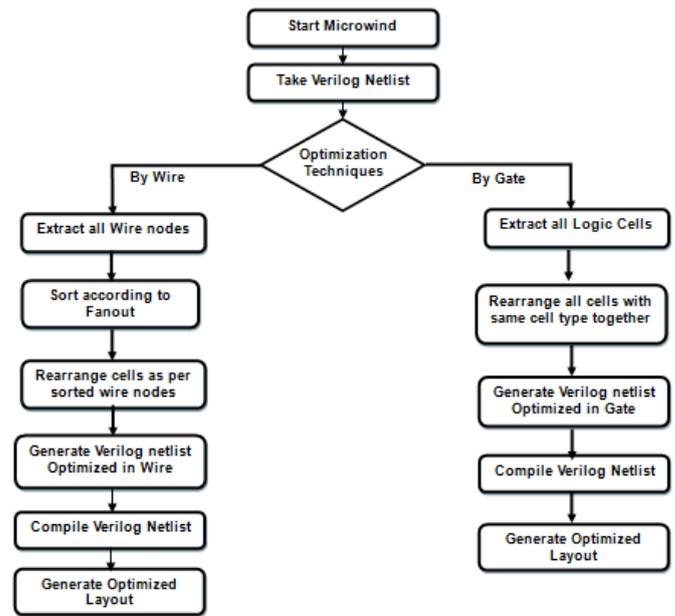


Fig 2: Flow Chart

Next step includes an optimization logic which is now implemented in MICROWIND Tool. Optimization logic will contain rearrangement of net list in two ways first is rearrange net list by wires and second is rearrange by logic cells i.e. gates. The algorithm of optimization logic is as follows:-

Firstly it takes original verilog net list from DSCH design and then extracts interconnect wire nodes from net list as it contains actual input-output information. Once all wire nodes are extracted, we will calculate the fan-out of each gate that means occurrence of each wire node. Then in next step select the node with the highest occurrence first and

locate its locations in net list and simultaneously place all those lines one after another to form an optimized net list by wires. This in turn will minimize total interconnect length as all gates with same wire node in their input or output will be placed together and also will keep more interconnect wires in same layer to minimize the total area.

Now the same optimization logic can be used to rearrange the net list by gates. Only the difference is that database contains all logic cells instead of interconnect wires that can be used in any design of DSCH and MICROWIND. This logic will bring same type of all logic cells together to form an optimized net list by gates. The advantage of this type of

rearrangement is that while observing the layout, an IC designer can easily distinguish between numbers of logic cells present in the layout.

Once the optimized net list by wire is generated then next step is to compile and generate its layout in MICROWIND software. If designer found that the layout generated is not much optimized then he can go back to rearrange net list stage and select rearrange by gate option to generate gate optimized net list. Again designer will compile and generate layout. By the practical observations it is found that 90% examples of MICROWIND are successfully optimizing by this logic.

#### 4. RESULTS & DISCUSSION

By using the methodology as described in above section, we have tested it for few examples and the results are as shown below-

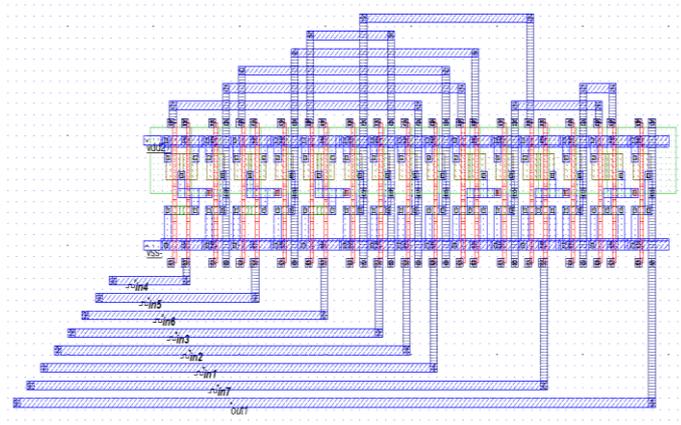


Fig 3: Four\_Bit\_ADC (Original Layout- with 6 layers in upper side)

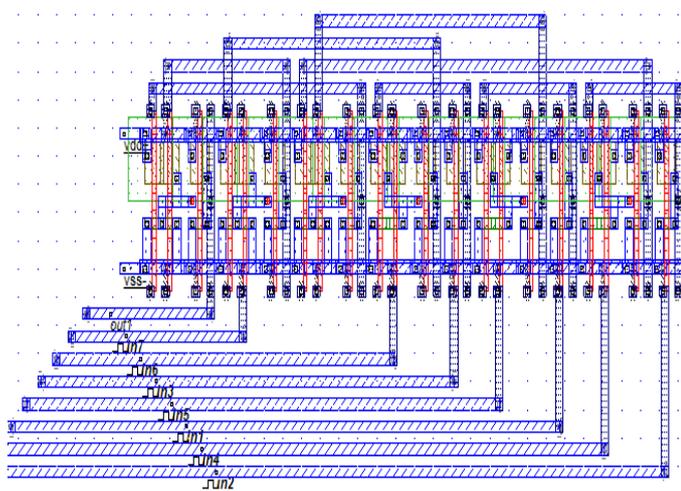


Fig 4(a): Optimized layout using WIRE rearranging logic- contains only 4 metal layers in upper side

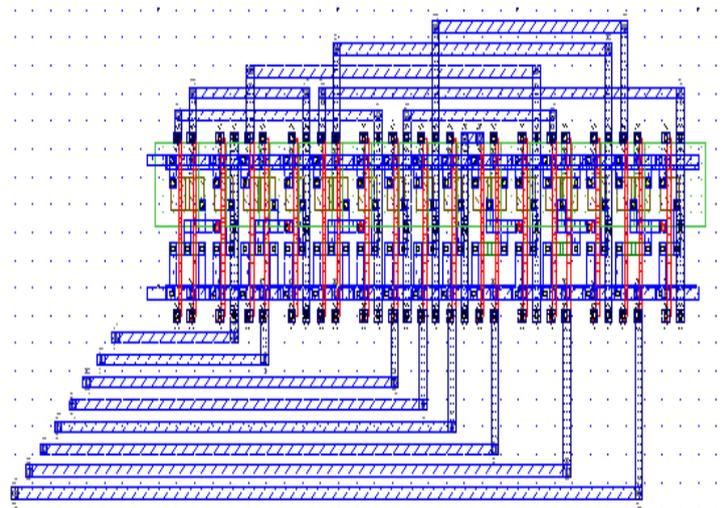


Fig 4(b): Optimized layout using GATE rearranging logic- contains 5 metal layers in upper side.

Fig 3 shows the original layout of a four bit ADC which contains total 6 layers in upper side of the PMOS and NMOS cells. After applying the optimization logic we can observe that the number of layers is minimized. As shown in fig 4 (a) when we apply the wire optimization logic layers are minimized to 4 and when we apply gate optimization logic the total number of layers are minimized to 5.

Table I: Optimization Results of Few More Examples

Circuits	Before		After Optimization			
	Optimization		By Wire		By Gate	
	Area ( $\mu\text{m}^2$ )	Metal Layers (Nos.)	Area ( $\mu\text{m}^2$ )	Metal Layers (Nos.)	Area ( $\mu\text{m}^2$ )	Metal Layers (Nos.)
Full						
Adder	205.7	5	183.4	3	183.4	3
ADC (4 Bit)	198.3	6	171.8	4	180.7	5
Counter(4 Bit)	601.6	5	528.7	3	601.6	5

In similar way we have tested few more examples and observed the changes in number of metal layers, total area and interconnect length which is mentioned in above table 1.

## 5. CONCLUSION

The verilog optimization logic of rearrangement of net list by wire and gate is working with the most of the examples tested by MICROWIND software. The results observed shows a drastic change in placement of cells and their interconnect routing. Eventually that will also optimize the total area and interconnect delay to increase the speed of operation as well as to improve the performance. This logic will be added in the upcoming version of MICROWIND software tool for better understanding of the CMOS IC layout designing concepts. The same algorithm of optimizing verilog net list can be applied to other educational software or EDA tools which uses the verilog net list for placement and routing.

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## BIOGRAPHIES

**Mahesh G. Jaiswal** PG Scholar in VLSI & Embedded systems, from Pimpri Chinchwad College of Engineering, Pune University, India. He has completed BE in Electronics and Telecommunications from Government College of Engineering & Research Pune, India in 2015. He is currently working with Ni Logic Pvt. Ltd Pune as software developer. His main research area of interest includes ASIC design, VLSI Chip design and EDA tool development.



**Varsha Bendre** is working as an Assistant Professor at Department of E&TC, Pimpri Chinchwad College of Engineering, Pune, affiliated to Savitribai Phule Pune University, Pune, India. She received her B.E. degree from Amravati University and M.E. degree from University of Pune in 2000 and 2010 respectively. Her research interest includes VLSI Design, Technology, Microelectronics, Low Power analog VLSI Design and Signal Processing.



**Vinay Sharma** is currently working as technical director at Ni Logic Pvt. Ltd. Pune, India since last 10 years. He has completed his M. Tech. in Digital Systems from College of Engineering Pune, India. Also he have B. Tech. Degree in Electronics from Shivaji University, India. His main area of research includes software developing, EDA tools based on ASIC design and VLSI Chip design concepts like MICROWIND, System Crafter and tools based wireless antenna design like CEM Solutions, 20-Sim and other products like 3D printer etc.