Power quality improvement and ripple cancellation in zeta converters

Mariamma John[1], Jois.K.George[2]

[1] *Student, Kottayam Institute of Technology and Science, Chengalam, Kottayam, India*
[2]Assistant Professor, Kottayam Institute of Technology and Science, Chengalam, Kottayam, India

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Abstract - *This paper presents a power factor corrected (PFC) zeta converters a cost effective solution for low power applications. In this work by adjusting the dc link capacitor voltage, we can use this converter for various low power applications. This paper deals with the implementation of pulse width modulated Zeta converter. A MATLAB/Simulink environment is used to simulate the model.*

***Key Words*: Zeta converter, Power factor correction (PFC)**

1.INTRODUCTION

Zeta converter topology provides a positive output voltage from an input voltage that varies above and below the output voltage. The zeta converter also needs two inductors and a series capacitor sometimes called flying capacitor. Unlike the SEPIC converter, which is configured with a standard boost converter, the zeta converter is configured from buck controller that drives a high-side P-MOSFET. The zeta converter is another option for regulating an unregulated input-power supply, like a low cost wall wart.

2. PFC BASED ZETA CONVERTER

2.1 Operation of Zeta converter

This converter is the latest type of single-stage input current shapers. It also uses single switching device and inherently provides an overload, short circuit, and inrush current protections. Since zeta converters behave as a resistive load to input AC mains, these converters are also called resistance emulators. Zeta converter is fourth order converters that can step down or step up the input voltage. The Zeta converter has many advantages, such as buck-boost capability, and continuous output current, input to output DC insulation, so it can be used in high reliability system. This topology offer high efficiency, especially by using the synchronous rectification. The synchronous rectification can be easily implemented in this converter, because this topology, unlike the SEPIC converter, uses a low-side rectifier. The equivalent circuit of the Zeta converter is in figure

The operation of an isolated zeta converter is classified into three different modes corresponding to switch turn-ON, switch turn-OFF, and DCM. Three modes are shown in Figure below and their associated waveforms are shown in Fig. 3. These modes are described as follows.

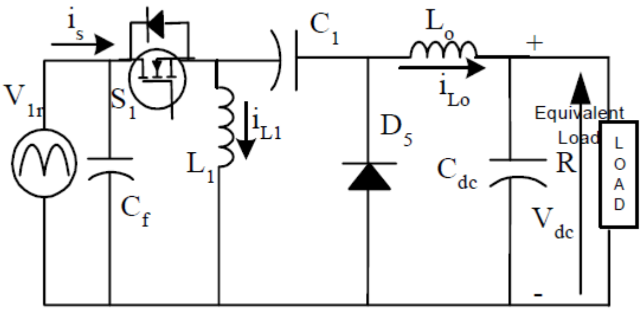


Fig -1: Equivalent circuit of zeta converter

Mode I: When switch (Sw) is turned "ON," a current in magnetizing inductance (Lm) of high frequency transformer (HFT) increases as shown in Fig. 2(a). Voltage V_{Lm} and V_{Lo}

Are equal to I_{in}.In this interval diode D is off with reverse voltage equal to $-(V_{in}+V_o)$. Inductor $L_m \& L_o$ get energy from voltage source and there respective currents increased linearly by $\frac{V_{in}}{L_m}$ and $\frac{V_{in}}{L_o}$.Switch current is increased linearly as $\frac{V_{in}}{L}$.The intermediate capacitor ($C1$) supplies energy to an output inductor (Lo) and the dc link capacitor (Cd). Hence, voltage across intermediate capacitor ($VC1$) reduces, and the current in output inductor (iLo) and dc link voltage (Vdc) are increased as shown in Fig. 3.

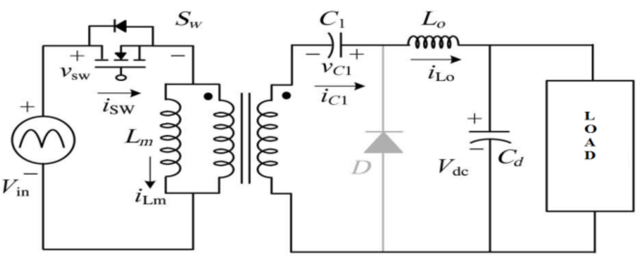


Fig -2: Mode-I operation of zeta converter.

Mode II: When switch (*Sw*) is turned "OFF," the current in magnetizing inductance (*Lm*) of HFT and output inductor (*Lo*) starts reducing. This energy of HFT is transferred to the intermediate capacitor (*C*1), and therefore voltage across it increases. Diode (*D*) conducts in this mode of operation, and the dc link voltage (*V*dc) increases as shown in Fig. 3.

Switch turns off diode D gets forward biased starting to conduct. Voltage across $L_m \& L_o$ become equals to $-V$o and the inductors $L_m \& L_o$ transfers energy to capacitor C1 and load. Current of $L_m \& L_o$ decreases linearly by a rate of $^{-V0}/_{Lm}$ & $^{-Vo}/_{Lo}$. Current in diode decreases at rate of $\frac{-Vo}{L}$.

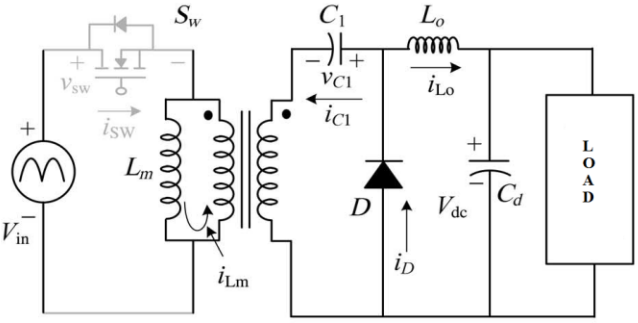


Fig -3:Mode-II operation of zeta converter

Mode III: This mode is DCM such that the energy of HFT Is completely discharged as shown in Fig. 2(c). The intermediate capacitor (*C*1) and the dc link capacitor (*Cd*) supply the energy to the output inductor (*Lo*) and the load, respectively. Hence, the dc link voltage (*V*dc) and intermediate capacitor's voltage (*V*C1) are reduced, and the output inductor current increases in this mode of operation as shown in FIGRE.

Due to extinction of diode circuit current, the diode circuit will behave as an open circuit &till that time switch Sw open. Capacitor current i_{c1} constant and equal to output inductor current i_{Lm} causing voltage at the inductor to be zero.

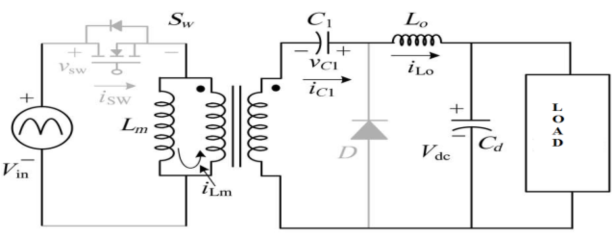


Fig -4: Mode-III operation of zeta converter.

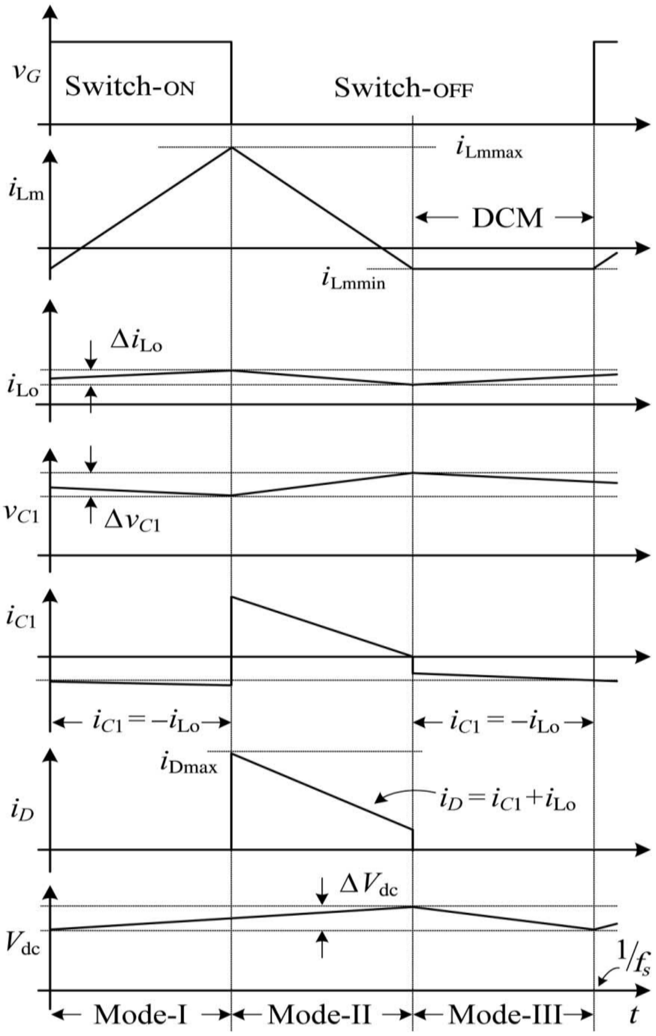


Fig -5: Different operating modes and there corresponding waveforms of zeta converter

2.2 Design of Zeta converter

An isolated PFC zeta converter is designed to operate in DCM such that the current flowing in magnetizing inductance of HFT (Lm) becomes discontinuous in a switching period.

The input voltage Vs applied to the PFC converter as $Vs(t) = Vmsin(w_L t)$ where Vm is peak input voltage and w_LL = $2\pi f_L$; f_L is the line frequency,i.e.,50 Hz.

The instantaneous output voltage of DBR is given as

$$Vin(t) = \left| V_m \sin\,(2\pi f_L t) \right|$$

where | | represents the modulus function. Output voltage V_{dc} of zeta converter

$$V_{dc} = \frac{N2}{N1}\frac{D}{(1-D)}V_{in}$$

where D represents the duty ratio and $\frac{N2}{N1}$ is the turns ratio of the HFT which is taken as $\frac{1}{2}$ The instantaneous value of duty ratio D(t) depends on the input voltage Vin(t) and required dc link voltage V_{dc}. An instantaneous duty ratio D(t) is

$$D(t) = \frac{V_c dc}{\frac{N2}{N1}V_{in}(t) + Vdc} = \frac{V_c dc}{\frac{N2}{N1}\left|V_m \sin(wt)\right| + V_{dc}}$$

The instantaneous power Pi at any dc link voltage (V_{dc}) is taken as linear function of V_{dc} as

$$Pi = \frac{Pmax}{V_{dcmax}}V_{dc}$$

where V_{dcmax} represents maximum dc link voltage and $Pmax$ is the rated power of the PFC converter. The critical value of magnetizing inductance of the HFT (Lmc) is expressed

$$Lmc = \frac{R_{L1} - D(t)^2}{2D(t)f_s \frac{N2}{N1}^2}$$

Where RL represents the emulated load resistance, fs is the switching frequency (which is taken as 20 kHz), and Pi is the instantaneous power. The expression for calculation of output inductor is as

$$Lo = \frac{V_{dc}(1 - D(t))}{f_S(KIo)}$$

Where k represents the percentage ripple of the output inductor current which is taken as 40% of output inductor current (k).

An expression for intermediate capacitor (C1) is

$$C1 = \frac{V_{dc}D(t)}{\eta\{\sqrt{2V_s} + V_{dc}\}}\frac{Pi}{V_{dc}^2}$$

where η is the permitted ripple voltage across intermediate capacitor and is 10% of VC1. The value of dc link capacitor (Cd) is calculated as

$$Cd = \frac{I_{dc}}{2w\Delta V_{dc}} = \frac{Pi}{V_{dc}}\frac{1}{2w(\eta V_{dc})}$$

Where ΔVdc represents the permitted ripple in dc link voltage η represents the percentage of permitted dc link voltage ripple.

A low-pass LC filter is used to avoid the reflection of higher order harmonics in supply system. The maximum value of filter capacitance (C_{max}) is given as

$$Cmax = \frac{Pmax}{w_L}\frac{\frac{\sqrt{2}}{V_S}}{\sqrt{2V_s}}tan\theta$$

Where θ is the displacement angle between the fundamental component of supply voltage and supply current which is taken as 1.

The value of filter inductor is given as

$$Lf = \frac{1}{4\pi^2 f_c^2 C_f} - 0.03\left(\frac{1}{w_L}\right)\left(\frac{Vs^2}{Po}\right)$$

where fc is the cutoff frequency which is selected such that $f_L < f_c < f_s$ .Therefore, f_c is taken as $f_s = 10$.

3. CONTROL OF ZETA CONVERTER

3.1 PI-Controller

A voltage-follower approach is used for the control of zeta converter. This control scheme consists of a reference voltage generator, voltage error generator, PI controller, and a PWM generator. A "reference voltage generator" generates a reference voltage Vdc. by multiplying the reference speed of BLDC motor (ω) with the voltage constant (kb) of motor as

$$V_{dc} = K_b * \omega$$

The "voltage error generator" compares the reference dc link voltage (Vdc) from reference voltage generator with the measured dc link voltage (V^*dc) to generate an error voltage (Ve) given as

$$V_e(k) = V_{dc}^*(k) - V_{dc}(K)$$

Where "k" represents the k th sampling instance. This error voltage Ve is given to a PI (proportional integral) controller to generate a controlled output voltage (Vcc) to PWM generator which is expressed as

$$V_{cc}(k) = V_{cc}(k-1) + K_p\{V_e(k) - V_e(k-1)\} + Ki(V_e(k))$$

Where Kp and Ki are the proportional and integral gains of the PI controller. Finally, the PWM signal for switch Sw is generated by comparing the output of PI controller (*Vcc*) with high-frequency saw-tooth signal (*mc*) given as

If *mc* < *Vcc*, then *Sw* = *"ON"*

If *mc* > *Vcc*, then *Sw* = *"OFF"*

Where Sw *represents* the gate signal to PFC converter switch ripple cancellation.

4. SIMULATION RESULTS

MATLAB software is used to evaluate the effectiveness of PI controller. Simulation parameter of zeta converter is given below table.

Table 1:parameters of zeta converter

Critical value of Magnetizing inductance	2.52mH
Output Inductor	4.2mH
Intermediate Capacitor	0.44
DC Link Capacitor	2200
Filter Inductor	3.77mH
Filter capacitance	330nF

4.1 Simulink Model of Closed Loop Zeta Converter

Figure shows the Simulink model of closed loop zeta converter. The proposed zeta converter controls the dc link voltage at set reference by controlling the duty ratio (D). Metal oxide field effect transistor (MOSFET) is employed as a switching device in zeta converter.

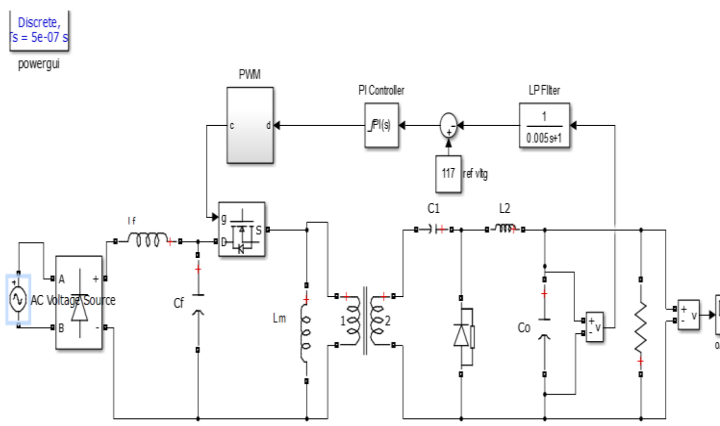


Fig -6: Simulation model of closed-loop zeta converter

The high frequency transformer (HFT) is used to the isolation between the input and output stages. It also provides flexibility for use of large voltage ratio. The control loop starts with sensing of dc link voltage and it's compared with reference dc link voltage. The error dc voltage is passed through a voltage of PI controller to give the modulating current signal and then compared with the saw-tooth carrier wave to generate the PWM switching pulse for the DC-DC converter.

4.2 output voltage waveform

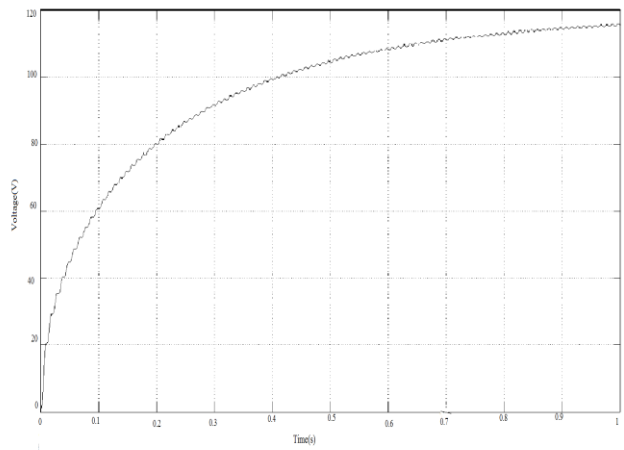
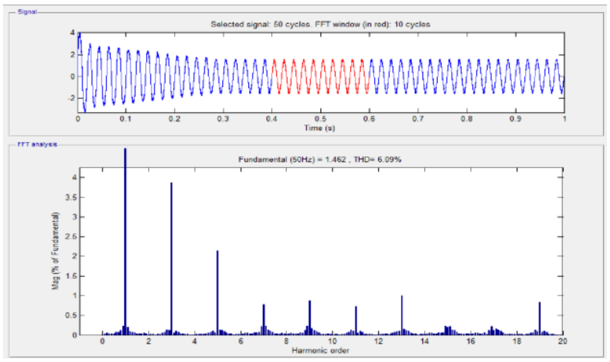


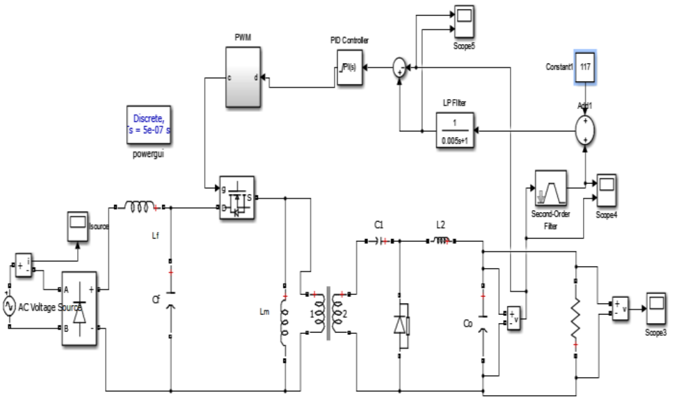
Fig -7: DC link voltage of zeta converter for given reference level.

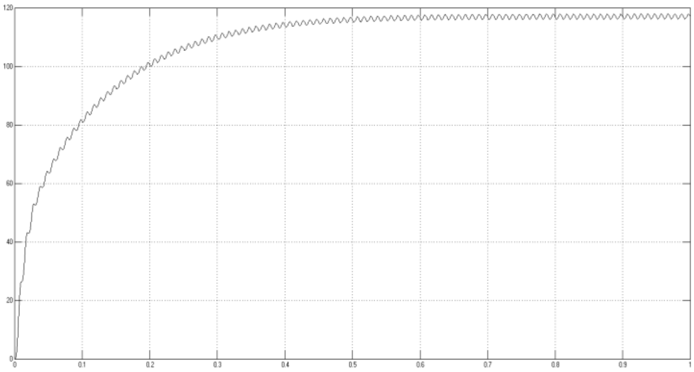
Figure shows the waveform of output voltage for closed loop system with a specific reference level. The output voltage is maintained at reference level.

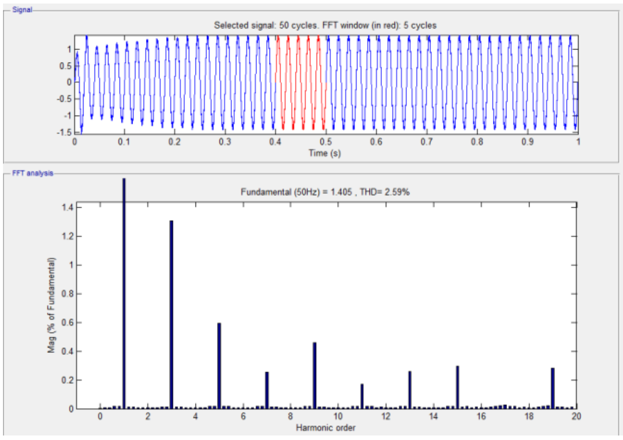


4.2 Simulink Model of Ripple Canceled Zeta Converter

Figure shows the Simulink model of closed loop ripple canceled zeta converter. Here the dc link voltage is filtered out by using a band pass filter and its added to the system voltage. Then its compared with the actual dc output of zeta converter. The error dc voltage is passed through a voltage of PI controller to give the modulating current signal and then compared with the saw-tooth carrier wave to generate the PWM switching pulse for the DC-DC converter.







4.3 Inference

System Configuration	THD
PI controlled ZETA converter	6.09%
Ripple canceled ZETA converter	2.59%

5. CONCLUSION

Zeta converter is another converter topology to provide a regulated output voltage from an input voltage that varies above and below the output voltage. The benefits of zeta converter over the SEPIC converter include lower output-voltage ripple and easier compensation. An isolated zeta converter is proposed for targeting low power applications.

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