International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 08 | Aug-2016 www.irjet.net p-ISSN: 2395-0072

Digital Implementation of Frequency and Phase Locked Loops

Anantha Shayanam G R[1], Dr. Santanu Sarma[2], Dr. Siva Yellampalli[3], Dr. J Krishna Kishore[4]

[1] *Anantha Shayanam G R, Department of ECE, VTU extension Center, UTL Technologies Bangalore Karnataka India/ Mobile (e-mail:ananthautl@gmail.com).Is with ISRO Satellite Centre working as research engineer Bangalore Karnataka India*

[2] *Dr. Santanu Sarma is with University of California Irvine, Irvine CA 92697, USA.*

[3] *Dr. Siva Yellampalli is with Department of ECE, VTU extension Center UTL Technologies Bangalore Karnataka India, (e-mail: siva.yellampalli@utltraining.com)*

[4] *Dr. J Krishna Kishore is with ISRO Satellite Centre working as senior scientist Bangalore Karnataka India, (e-mail:jkk40@yahoo.co.in)*

Abstract - *Real time estimation of frequency, phase and magnitude of a pure sinusoidal signal is a classical problem that has many practical applications. Phase looked loops are widely used in these applications, but using PLL in these applications is more costly. The novel approach of designing Adaptive Frequency and Phase Locked Loop (FPLL) for these applications is proposed and discussed. This paper presents the digital implementation of Adaptive Frequency and Phase Locked Loop (FPLL) and also aims at in detail deliberation of simulation. The logics of adaptive FPLL is realized in digital domain using VHDL and the inevitable complications of algebraic loop in closed loop algorithm are addressed. Also given suggestion for selecting the number system for the practical DSP applications and discussed the implementation issues of closed loop algorithms in the z-domain compared with the s-domain.*

Key Words: FPLL, Algebraic loop, Adaptive PLL, Fixed Point, Floating Point, Digital implementation, CORDIC algorithm, VHDL.

1. INTRODUCTION

Adaptive Frequency and Phase locked loop [1, 2] will provide parallel estimation of frequency, phase and magnitude of pure sinusoid. We can use in speed and position estimation using the angular sensors and also in the demodulators, frequency synchronizers ext. The FPLL has a better tracking performance due to adaptive frequency estimation and update law and is more computationally efficient as compared to a secondary order phase locked loop [3] and Costas loop [4] and wide bandwidth. Unlike conventional and Costas PLL, it has simple structure. The simulation of Adaptive FPLL in the s-domain is carried out and translated the system from S-domain to Z-domain, compared the performance of the system in s domain and z domain and implementation of the digital FPLL in the digital domain using VHDL is discussed.

2. Working Principle and Design Architecture

The basic operation principle of the adaptive FPLL is, placing the poles in the imaginary axis of the s-domain and moves the location of the poles in imaginary axis by estimating the frequency difference between input and the oscillating loop frequency in the structure. The estimated error feedback to change oscillating loop frequency this keeps

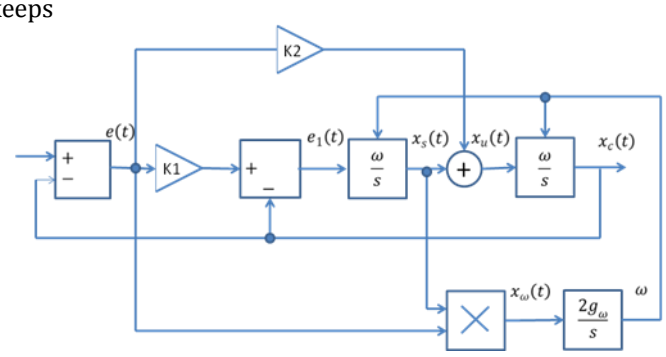

Fig -1: Structure of Adaptive Frequency Phase Looked Loop

Continue until the input frequency and estimated frequency becomes equal. The main reason to consider this algorithm is because of the simple structure and the bandwidth as compare to PLL. As s-domain simulation shows that bandwidth is theoretically infinite. In the digital implementation the bandwidth of the Adaptive FPLL is dependent on the sampling frequency for the upper cutoff frequency. Adaptive FPLL architecture consists of two loops which are used for the controlling the internal oscillations and to steer the oscillating loops frequency towards the input signal frequency. The figure.1 shows the structure of the adaptive FPLL and the performance of frequency and amplitude convergence of the FPLL which is depended on the parameters K1, K2 and Gw. The values of the mentioned parameters shall be optimally chosen for particular frequency bands. In this paper simulation of Adaptive FPLL is done in both in analog domain and digital domain.

3. Analog and digital analysis and simulation of FPLL

The simulation of Adaptive FPLL is carried out in analog domain and the digital domain and the specification and results are presented below. Parameters K1, K2 and Gw are the variables in algorithm. By changing the values of K1, K2 and Gw we can see the performance variation in both frequency and amplitude convergence. The variable Gw is appears in the frequency estimation loop as the value of Gw increases, the frequency convergences time reduces.

The internal oscillating loop is producing the quadratic signal. The characteristic equation for the I-phase and Q-phase components are shown in equation 1 and 2 as given in reference 1.the figure 3 shows the bode plot for the transfer functions at k1 and k2 value is one.

I-phase component:

$$TF_I = \frac{w(k_2 s + w * k_1)}{s^2 + wk_2 s + (k_1 + 1)w^2} \quad (1)$$

Q-phase component:

$$TF_Q = \frac{w(k_1 s - w * k_2)}{s^2 + wk_2 s + (k_1 + 1)w^2} \quad (2)$$

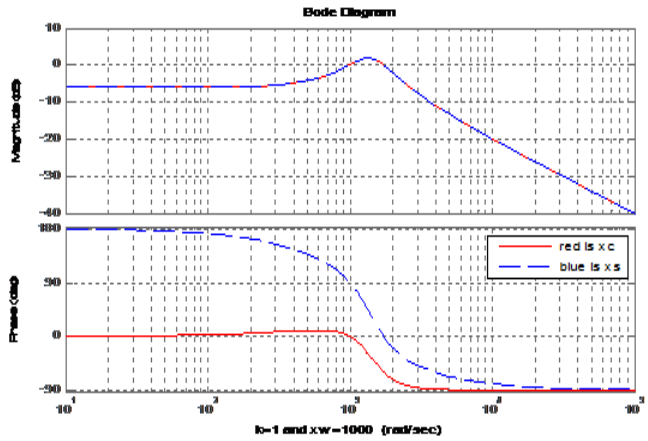

Fig -2: Bode plot of transfer function at k1=k2=1

3.1 Analog simulation

Specifications:

1. Input frequency: 1 – 200 KHz.
2. Gw=100;
3. K=10.
4. Initial xw=2.*pi *1 rad/sec;

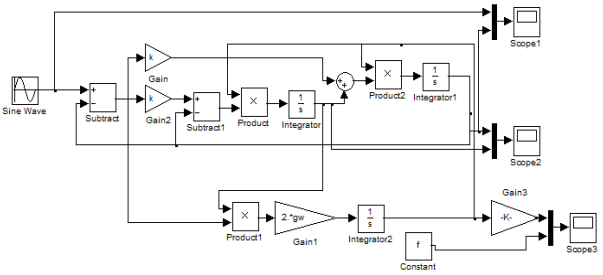

Fig -3: Simulink model of Analog FPLL

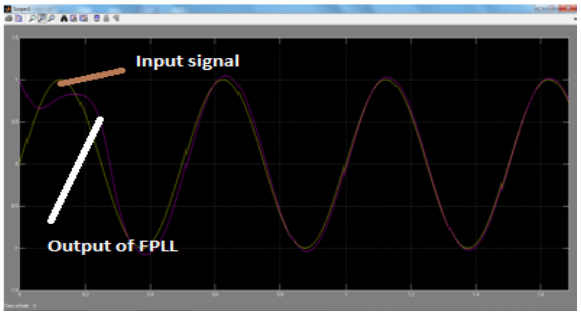

Fig -4: Input and output of FPLL

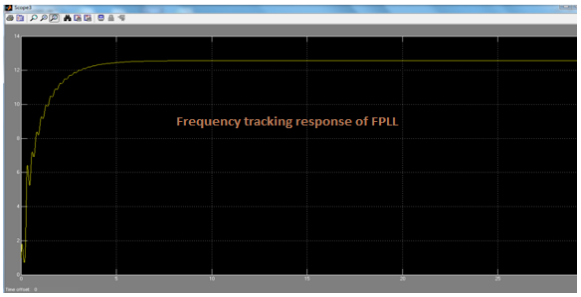

Fig -5: Estimated Frequency output

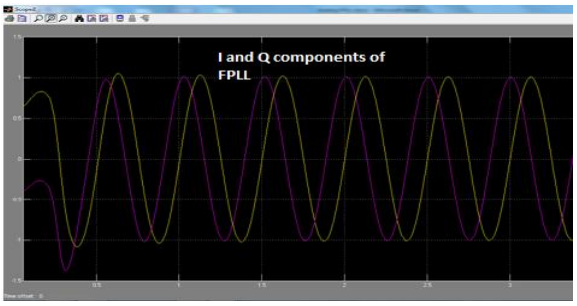

Fig -6: I and Q component of FPLL

3.2 FPLL as FSK Demodulator

As mentioned above Adaptive FPLL fits into many applications such as in resolvers, frequency and phase estimation circuits, synthesizers and demodulators. One of the straight forward applications of Adaptive FPLL is in the frequency demodulators i.e., based band FSK demodulators without doing any modifications to the architecture and simulations results are presented below. Figure 7 shows the simulink simulation model "1" represented as frequency of 5.5 KHz and "0" is represented as 2.5 KHz and bit rate of 100 bits/sec.

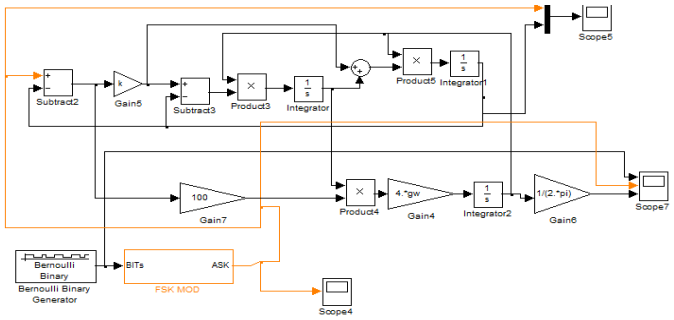

Fig -7: Simulink model FSK Simulation

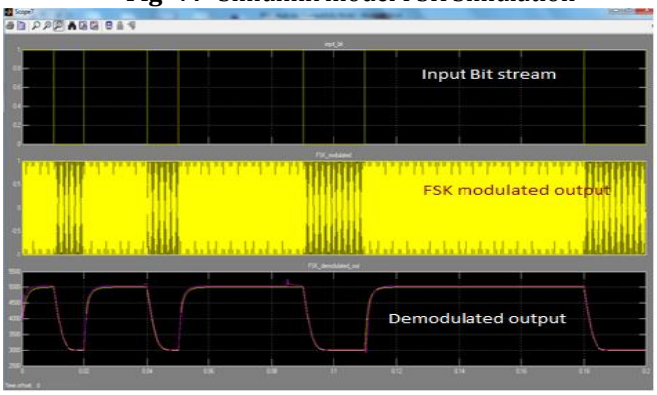

Fig -8: Simulink simulation of FSK modulation and demodulation

3.3 Digital simulation

There are many methods are available to convert system from the Laplace domain to the z- domain in that bilinear transformation is used because of closed approximation.

In bilinear transformation S-function is replaced with

$$S = \frac{2(1-Z^{-1})}{T_s(1+Z^{-1})}$$ Where Ts is the Sampling frequency.

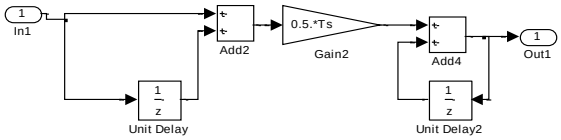

Fig -9: Z-domain representation of Integrator

Specification:

1. Input frequency: 1 – 200 KHz.
2. Gw=100;
3. K=10.
4. Inital xw=1 Hz;
5. Xc=1;
6. Xs=1;

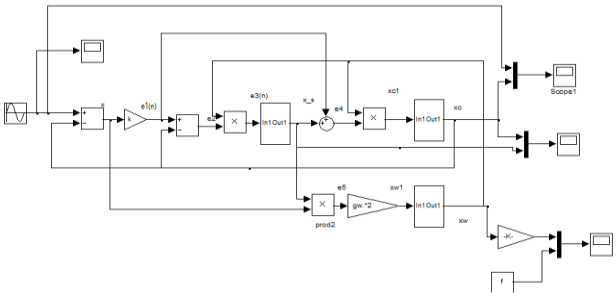

Fig -10: Simulink model of Digital FPLL

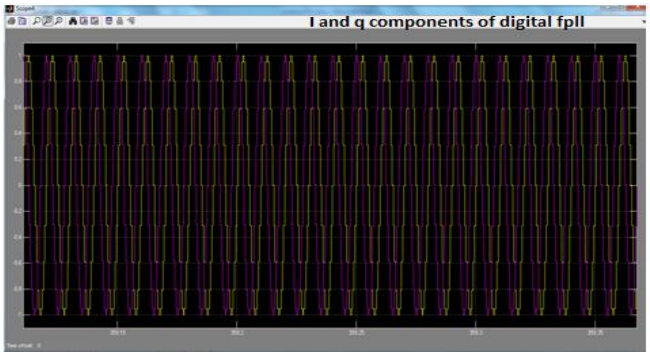

Fig -11: I and Q component of FPLL output

In the closed loop continuous system the output is fed back to the input to nullify the error. While converting this system to digital domain it is not possible to break the loop back path, this kind of loops called as an algebraic loops. There are various methods break the algebraic loops, like introducing the memory element in the feedback path but it may changes the dynamics of the system. As shown in the figure 12 for negative feedback continuous system to find values of the variable in the time domain i.e.,

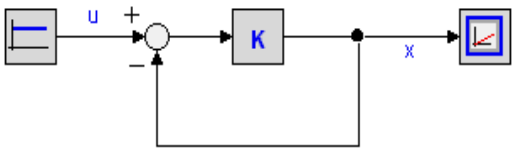

Fig -12: Illustration of Algebraic Loop

$$X= (U-X)*K$$

The values of X depends on its own value of X this can solved by rearranging the equation by

$$X=U*K/ (1+K)$$

In some of the cases it may not be possible to break loop without disturbing the loop dynamics in such cases the fixed error will exist in the output. As per the literature survey they are many methods to eliminate the algebraic loop some of them are listed below.

1. One of possibility of occurrence of Algebraic Loop is the random order of calculations. One can change the calculation order by rearranging the equation is one possibility of eliminating algebraic loop.

2. Introducing energy or memory storage elements to eliminate an algebraic loop. This results in the change in the dynamics of the equation and results in the fixed error at the output.

3. Reducing the number of variables or Combination of dual elements. Sometimes number of loops can be eliminated by adding the parameter values. Example the mass M1 and M2 can be combined by adding M1 and M2. However when reducing the number of elements by deletion care should be taken such they will not affect while deploying the system it may give proper results while doing simulation

But in our case algebraic loop is inherent and it's not possible to eliminate just by re-arranging the expression. We need to introduce a delay element. Because of extra delay element in the Simulink model results in the changes in the dynamics. We can avoid the effect of algebraic loop by increasing the sampling frequency.

3.4 Digital simulation

The prototyping of algorithm in the digital domain is carried out using VHDL, VHDL is considered to be strongly typed languages compared to other hardware description languages. As already mentioned that in order to break the algebraic loop the delay element is introduced in the feedback path results in error in the frequency estimation around 0 to 8% as the frequency increases the error in the estimation increases.

One of the main challenging jobs to implement DSP algorithms in the hardware such as the FPLL, the main requirement is number system representation and the precision we consider at each stage of the implementation. Number representation scheme for variables and constants in algorithm places major role in terms of efficiency of area and time, accuracy of the computation. Floating and Fixed point number representation schemes are considered initially in the designing stage and finally because of complexity of floating point representation and considering other facts such as to achieve the required efficiency in terms of time, area and accuracy, variable fixed point representation scheme at different places of implementation is selected. After the each arithmetic operation result is truncated to the appropriate format. We used 40bits to represent the data at any point of time in the algorithm. Where algorithm demands for more precision in the fraction part we used the convention of 4.36 fixed point formats. And where precision required for integer part we used the 24.16 format.

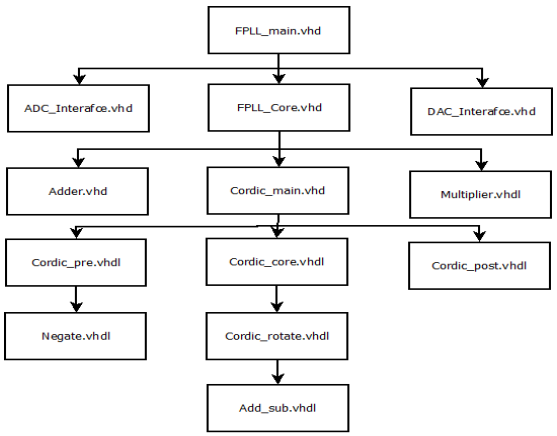

Fig -13: Architecture VHDL code architecture

The figure 13 shows the architecture of VHDL implementation of FPLL. Figure.14 shows the algorithm flow of Adaptive FPLL implementation in the FPGA. The sampling frequency considers is 20 times more than the maximum frequency of input signal. As depicted in the algorithm the incoming signal is sampled and fed to the frequency estimation loop mean while frequency generation loop oscillating at the initial set frequency, the error estimation output is from frequency estimation loop fed to the frequency oscillation loop results in increasing and

decreasing of the oscillating loop frequency and this continuous and once frequency locks to incoming signal, the locking indication is provided and CORDIC algorithm is used to measure the phase. The figures 15 and 16 show the simulated output results of FPLL in the Modelsim.

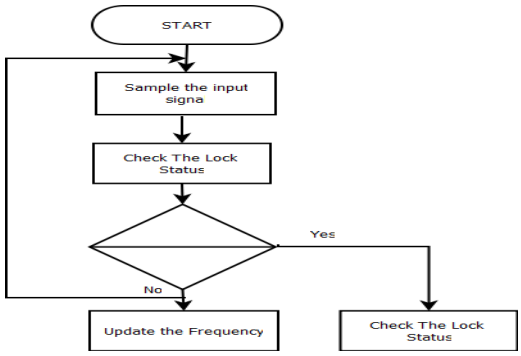

Fig -14: Algorithm of FPLL design in Hardware

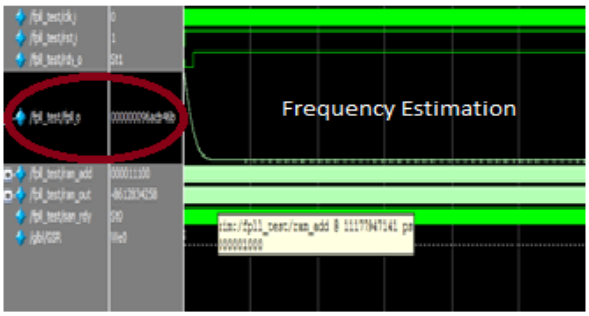

Fig -15:Frequency estimation in Modelsim

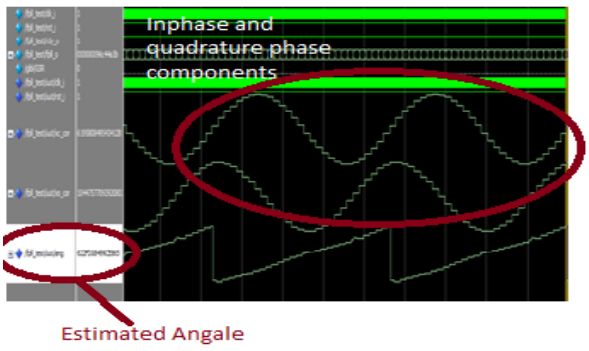

Fig -16: output of FPLL in Modelsim

4. Results

Table 1 shows the comparison results obtained in simulation of analog and digital domain in the SIMULINK and results obtained in hardware implementation in the FPGA. The error in the hardware implementation is considered to be more comparatively to fixed point simulation. the frequency estimation error of maximum 8% up to 200Khz.the factors to be consider for this error is the sampling frequency, truncation of computed results in the fixed point operations and the Size of the ADC.

Table -1: comparison of frequency estimation in different Domains

Sl. no	Input frequency In Hz	Frequency estimated in AFPLL	Frequency estimated in DFPLL	Frequency Estimated in the Hardware
1	700	700.1	699.5	691.52
2	1300	1300.1	1298.9	1272
3	3500	3500.02	3513	3260
4	6500	6500.05	6470	5788
5	7000	7000.05	6920	6439
6	70000	70000	71250	64278
7	700000	700000	692370	642533

Device Utilization Summary (estimated values)		
Logic Utilization	Used	Available
Number of Slices	2762	15640
Number of Slice Flip Fops	3374	33280
Number of 4 input LUTs	4974	33280
Number of bonded ICBs	244	519
Number of GCLKs	1	24
Number of DSP48s	48	84

Fig -17: resource utilization of FPGA

5. CONCLUSIONS

In this paper simulation of adaptive FPLL in s-domain and z-domain is carried out, digital implementation of adaptive FPLL was discussed and method to convert the system from s-domain to z-domain and problem of algebraic loops and number representation schemes and the estimation errors due to conversion methods were discussed and presented. Introducing the delay element to break algebraic loop cause the change in the dynamics of the system slightly and following are points derived from experimental results

1. Because of introducing the delay element in the feedback of the FPLL causing the frequency estimation error of maximum 8%.
2. The error is high for the high frequencies in the specified band width.
3. In the entire design we consider the sampling frequency 20 times greater than the highest input signal frequency.
4. If increasing sampling causing the frequency estimation closer to the input signal frequency.

The future work is focused on much more regressive study on the algebraic loops and reduces the effect of algebraic loop in the frequency estimation.

6. REFERENCES

[1] Santanu Sharma .2013,"Adaptive Technique for Computationally Efficient Time Delay and Magnitude Estimation of Sinusoidal Signals". https://www.researchgate.net/publication/255731159_Adaptive_Technique_for_Computationally_Efficient_Time_Delay_and_Magnitude_Estimation_of_Sinusoidal_Signals.

[2] Santanu Sharma .2008,"Frequency and Phase locked loop using adaptive phase detectors", Australian Journal of Electrical & Electronics Engineering, Vol 4 No 3.

[3] Best, R. E. 1997, Phase-locked loops: Design, Simulation, and Applications. New York: McGraw-Hill, third ed.

[4] Roshna T R., Nivin R, Sherly Joy and Apren T J, "Design and implementation of digital Costas loop and Bit synchronizer in FPGA for BPSK demodulation ", Control Communication and Computing (ICCC), 2013 International Conference , pp. 39 – 44., ISBN 978-1-4799-0573-7.

[5] Chun, B., Lee, Y. H. and Kim, B. 1997, "Design of variable loop gains of dual-loop DPLL", IEEE Transactions on Communications, Vol. 45, No. 12, pp. 1520-1522.

[6] Gardner, F. M. 1979, Phase Lock Techniques. New York: John Wiley & Sons, Second ed., ISBN 0-471-04294-3.

[7] X. Wang and B. E. Nelson, "Tradeoffs of designing floating-point division and square root on virtex fpgas," in Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines, (Napa Valley, CA), pp. 195–203, April 2003.

[8] Izadi M.H. and Leung, B. 2002, "PLL-based Frequency discriminator using the loop filter as an estimator," IEEE Transactions On Circuits And Systems – Ii: Analog And Digital Signal Processing, Vol. 49, No. 11, pp. 721-727.

[9] Štukjunger, P.: Arithmetic in FPGA, Diploma thesis, CTU in Prague, 2004

[10] Lindsay, W. and Chie, C. M. 1982, "Performance measures for phase-locked loops-A tutorial", IEEE Transactions on Communications, Vol. Com-30, No. 10, pp. 2224-2227.

[11] Lu, J. 1999, "Broadband noise reduction using digital phase-locked loop", M. S. Thesis, The University of Toledo.

[12] Patapoutian, A. 1999. "On phase-locked loops and Kalman fi lters," IEEE Transactions on Communications, Vol. 47, No. 5, pp. 670-672.

[13] Piqueira, J. R. C. and Monteiro, L. H. A. 2003, "Considering second-harmonic terms in the operation of the phase detector for second-order phase-locked loop", IEEE Transactions On Circuits And Systems – I: Fundamental Theory And Applications, Vol. 50, No. 6, pp. 805- 809.

[14] Shahruz, S. M. 2002, "Novel phase-locked looped with enhanced locking capabilities", Proceedings of American control conference, May, Anchorage, pp. 4086-4091.