

Data converters for Scalable CMOS mixed signal Systems for VLSI

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Abstract – Data Converters are one of the circuits that belong to nonlinear category of analog and mixed signal circuits. The presented paper discusses data converter fundamentals, various DAC and ADC architectures and methods to implement those. Previously digital circuits form the basis of two discrete amplitude levels based circuits and systems. Nonlinear circuits are not purely analog or digital. These circuits belong to the category of mixed signal circuits where the inputs are not linearly related to outputs. Data converters a circuit that changes analog signals to digital representations or vice versa play an important role in an ever-increasing digital world. As more products perform calculations in the digital or discrete time domain, more sophisticated data converters must translate the digital data to and from our inherently analog world. This paper introduces concepts of data conversion and sampling which surround vast category of Data converter circuits.

Key Words: Data converters, ADC, DAC, Architectures of ADC and DAC,

1.INTRODUCTION

Analog-to-digital converters, also known as A/Ds or ADCs, convert analog signals to discrete time or digital signals. Digital-to-analog converters D/As or DACs perform the reverse operation. Data converters comprises of both ADCs and DACs and they are the most important integral parts of any power system. Since MOSFETS do form the system of any modern analog, digital or any mixed signal design at a certain abstraction level, Power MOSFETS and amplifiers made out of those will be the basis of any data converters that are exclusively meant for signal processing. One of the most popular data converters is Delta sigma converters also known by different names such as Oversampling ADC and most importantly noise shaping data converter. The above mentioned name comes from the architecture of modulator which integrates the difference between the input and quantized output.

Analog-to-digital or digital to analog converters play an essential role in modern RF receiver design. Conventional Nyquist converters require analog components that are precise and highly immune to noise and interference. In contrast, oversampling converters can be implemented using simple and high-tolerance analog components. Moreover, sampling at high frequency eliminates the need for abrupt cut-offs in the analog antialiasing filters. [2] A technique of noise shaping is used in SD converters in addition to

oversampling to achieve a high-resolution conversion. A significant advantage of the method presented in the paper is that analog signals are converted using simple and high-tolerance analog circuits, usually comparators, and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter.

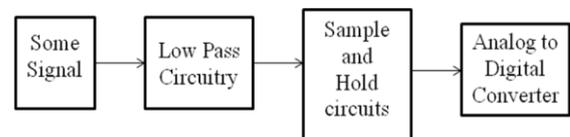


Figure 1 Signal characteristics changes in Analog to Digital conversion

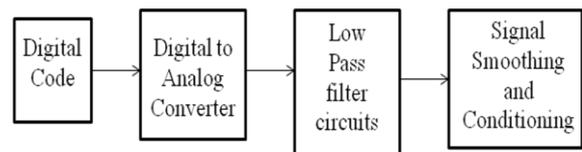


Figure 2 Signal characteristics changes in Digital to Analog conversion

Analog-to-digital converters, also known as A/Ds or ADCs, convert analog signals to discrete time or digital signals. Digital-to-analog converters (D/As or DACs) perform the reverse operation. Above two block diagrams illustrate these two operations. [1-7] To understand the functionality of these data converters, it would be wise first to compare the characteristics of analog versus digital signals. the original analog signal is filtered by an anti-aliasing filter to remove any high-frequency components that may cause an effect known as aliasing. The signal is sampled and held and then converted into a digital signal. Next the DAC converts the digital signal back into an analog signal. Note that the output of the DAC is not as "smooth" as the original signal. A low-pass filter returns the analog signal back to its original form plus phase shift introduced from the conversions after eliminating the higher order signal components caused by the conversion. This example illustrates the main differences between analog and digital signals. Whereas the analog signal in 1.1a is continuous and infinite valued, the digital signal in 1.2 is discrete with respect to time and quantized. The term continuous-time signal refers to a signal whose response with respect to time is uninterrupted. Simply stated, the signal has a continuous value for the entire segment of time for which the signal exists. By referring to the analog signal as infinite valued, we mean that the signal can possess any value between the parameters of the system.

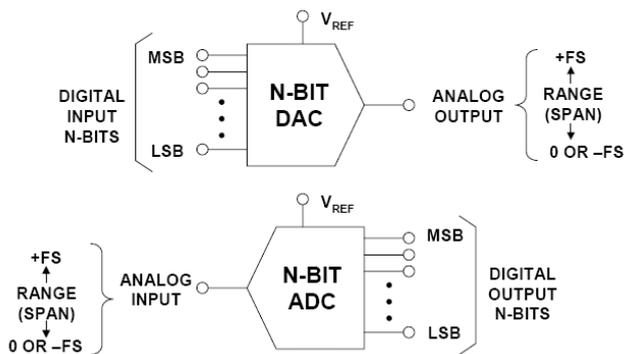


Figure 3 Fundamental block diagram for n-bit ADC and DAC

2. Data Converter Architectures

B Applications such as wireless communications and digital audio and video have created the need for cost-effective data converters that will achieve higher speed and resolution. The needs required by digital signal processors continually challenge analog designers to improve and develop new ADC and DAC architectures. There are many different types of architectures, each with unique characteristics and different limitations. This section presents a basic overview of the more popular data converter architectures and discusses the advantages and disadvantages of each along with their limitations. The basic architectures will be discussed using a top-down approach. Because many of the converters use op-amps, comparators, and resistor and capacitor arrays, the top-down approach will allow a broader discussion of the key component limitations in later sections.

A wide variety of DAC architectures exist, ranging from very simple to complex. Each, of course, has its own merits. Some use voltage division, whereas others employ current steering and even charge scaling to map the digital value into an analog quantity.

In many cases, the digital signal is not provided in binary code but is any one of a number of codes: binary, BCD, thermometer code, Gray code, sign-magnitude, two's complement, offset binary, and so on. For example, it may be desirable to allow only one bit to change value when changing from one code to the next. If that is the case, a Gray code will suffice. Notice that it requires $2N - 1$ bits to represent an N -bit word. The choice of code depends on the application, and the reader should be aware that many types of codes are available.

A survey of the field of current A/D converter research reveals that a majority of effort has been directed to four different types of architectures: pipeline, flash-type, successive approximation, and oversampled ADCs. Each has benefits that are unique to that architecture and span the spectrum of high speed and resolution. Since the ADC has a continuous, infinite-valued signal as its input, the important analog points on the transfer curve x-axis for an ADC are the ones that correspond to changes in the digital output word. These input transitions determine the amount of INL and DNL associated with the converter.

Flash or parallel converters have the highest speed of any type of ADC. Generally, the use of one comparator per quantization level ($2^M - 1$) and $2N$ resistors a resistor-string DAC). The reference voltage is divided into $2N$ values, each of which is fed into a comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators. A thermometer code exhibits all zeros for each resistor level if the value of v_m is less than the value on the resistor string, and ones if v_m is greater than or equal to voltage on the resistor string. A simple $2N - 1:N$ digital thermometer decoder circuit converts the compared data into an N -bit digital word.

The obvious advantage of this converter is the speed with which one conversion can take place. Each clock pulse generates an output digital word. The advantage of having high speed, however, is counterbalanced by the doubling of area with each bit of increased resolution. For example, an 8-bit converter requires 255 comparators, but a 9-bit ADC requires 511. Flash converters have traditionally been limited to 8-bit resolution with conversion speeds of 10-40 Ms/s using CMOS technology. The disadvantages of the Flash ADC are the area and power requirements of the $2N - 1$ comparator. The speed is limited by the switching of the comparators and the digital logic.

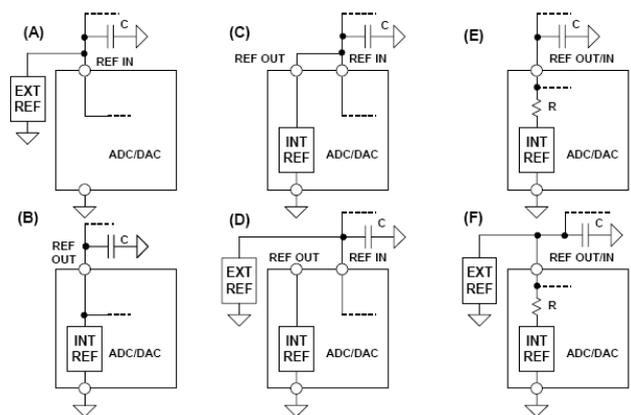


Figure 4 Popular ADC/DAC reference options[5]

3. Implementing Data Converters

Technology continues to scale towards smaller dimensions. This feature size reduction is driven mainly by the desire to implement digital systems of increased complexity in a smaller area. This natural trend in feature size reduction, with accompanying reduction in supply voltage and poorer matching, can present challenges for the CMOS circuit designer. The accompanying lower supply voltage, for example, results in an inherent reduction in dynamic range, decrease in SNR, and increasing challenges when implementing analog circuitry with little, ideally zero, voltage overhead.

This section reviews and discusses implementation methods and trade-offs for designing data converters in nanometer CMOS. For DAC design, we focus on converters

implemented with both resistors using R-2R networks and current sources. The benefit of, and reason we are focusing on, using R-2R networks and current sources over other methods for DAC implementation, such as charge redistribution DACs, is the absence of good poly-poly capacitors in nanometer digital CMOS processes. R-2R-based DACs can be laid out in a small area while achieving resolutions in excess of 10-bits without calibrations or trimming. Charge-scaling DACs require linear capacitors. The layout area needed for these capacitors can often be very large and practically limit both the resolution and accuracy of the DAC. It's important to note that the goal in this paper is not to provide an exhaustive overview of data converter design but rather to provide discussions and practical insight helpful when implementing any type of data converter in SCMOS technology.

4. Previous Works

Angsuman Roy and R. Jacob Baker in their paper entitled, "A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion" designed a passive 2nd-order sigma-delta modulator based on a cascade of first-order lowpass filters was designed, fabricated, and tested. A lumped RC filter is added in the loop of a conventional 1st-order passive sigma-delta modulator in order to improve the linearity of its transfer function. A low power edge-triggered comparator was designed and fabricated along with lumped components in ON Semiconductor's C5 500-nm process. The implementation achieved a THD below 1% for all frequencies between 10 Hz and 5 kHz. With a 5 V supply the power consumption of the sigma-delta modulator is 64.5 uW to 150 uW depending on the input signal. They concluded the low power sigma delta modulator presented in their paper retains relatively good precision despite the elimination of the active-integrator to reduce power dissipation. Although the linearity isn't as good as a sigma delta modulator implemented using an active integrator, the presented circuit should find use in applications which heavily prioritize power consumption and don't require high precision. Although the modulator was implemented in a 500-nm CMOS process the concepts presented should scale to smaller, lower-power, processes.

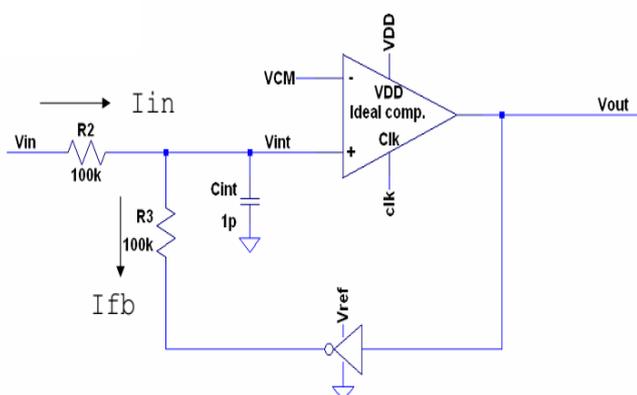


Figure 5 A 2nd order sigma delta modulator [1]

Angsuman Roy and R. Jacob Baker in their paper entitled, "A Low-Power Switched-Capacitor Passive Sigma Delta Modulator" presented a passive 2nd-order sigma-delta modulator using switched-capacitor based filters was designed, fabricated, and tested. A novel 2nd-order single feedback path topology is used. All circuitry is optimized for low power operation through the use of minimum size MOSFETs, component reduction and topology choice. The modulator was fabricated in On Semiconductor's C5 500-nm process. The implementation achieves a typical SNDR of above 50 dB for tested frequencies of 10 Hz to 3 kHz and has a peak SNDR of 57.8 dB, which corresponds to an ENOB of 9.3 bits. With a 2.5 V supply, the power consumption of the sigma-delta modulator is 6.75 μW. The modulator achieves a FOM of 1.78 pJ/step. They concluded that the Σ-Δ modulator proposed in their paper offers good resolution suitable for a nominal 10-bit ADC while consuming less than 10 μW of power for a typical range of clock frequencies. The presented circuit should find use in a wide variety of applications where limiting power consumption is the highest priority. Furthermore, the implementation in a 500-nm CMOS process allows IC designers restricted to older processes to further reduce power and remain competitive with newer CMOS processes. A suitable application for this Σ-Δ modulator is in battery-powered medical electronics since the C5 process on which it is implemented is qualified for medical use. The design presented should scale well to smaller processes and allow for even greater reduction in power consumption.

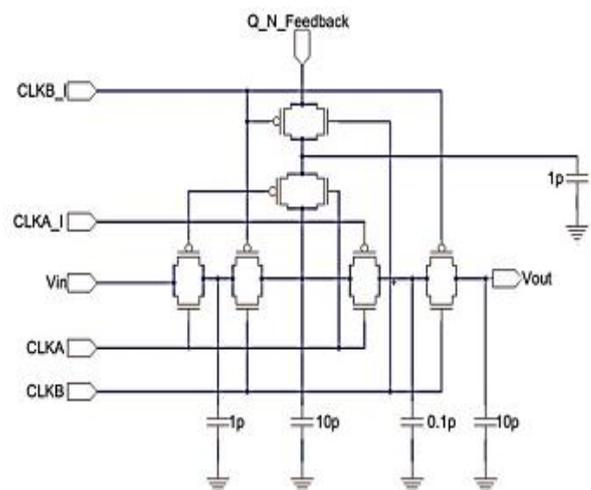


Figure 6 Schematic of switched-capacitor filter block

5. Work done till now

Various sections and subsections has been designed for the proposed work. The work includes modulator section, an integrator section and switched capacitor section as shown in previous work. The presented work also includes the design of amplifier which is as shown

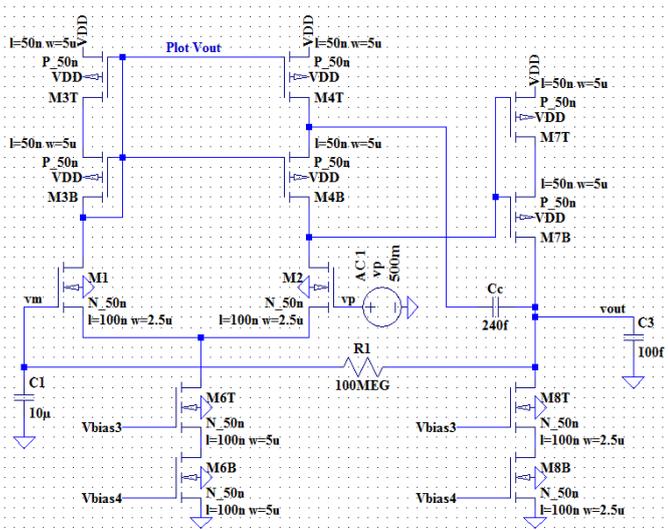


Figure 7 Operational amplifier design for Data Converters

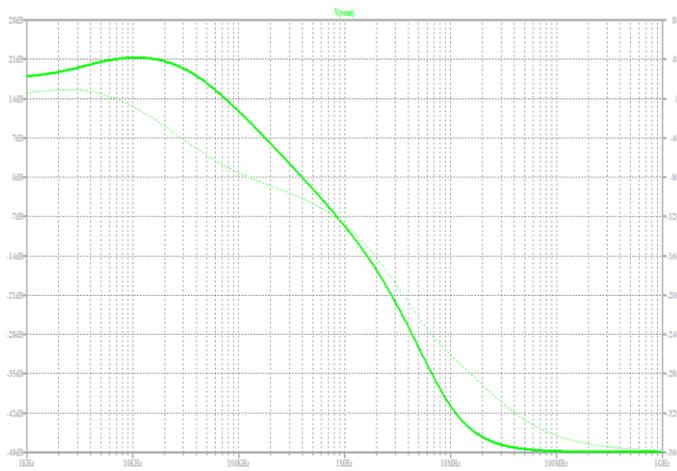


Figure 8 AC Response plot for Operational Amplifier (Operation Range - 1 GHz)

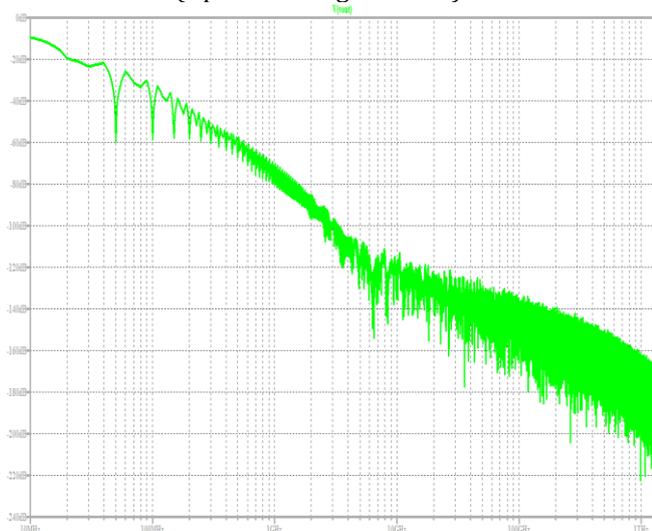


Figure 9 FFT for figure 6 AC response

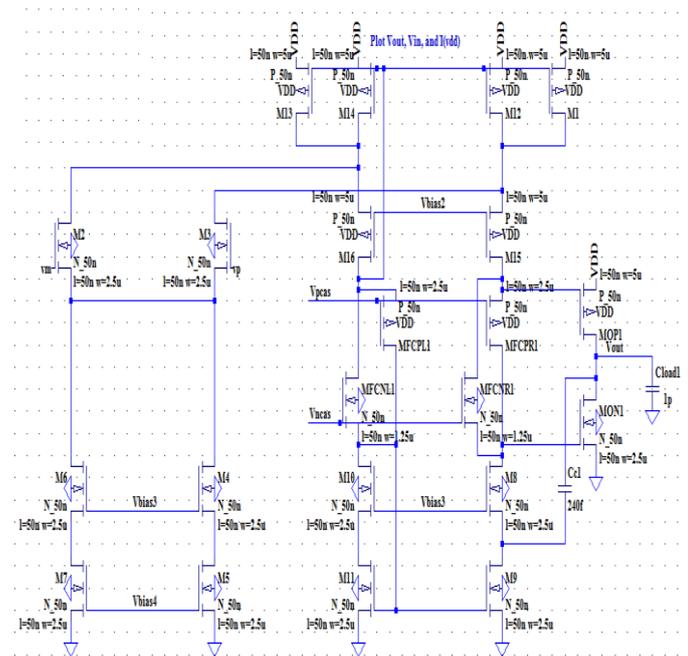


Figure 10 Operational Amplifier topology 2



Figure 11 Transient analysis for topology 2



Figure 12 FFT plot for transient analysis of amplifier topology 2

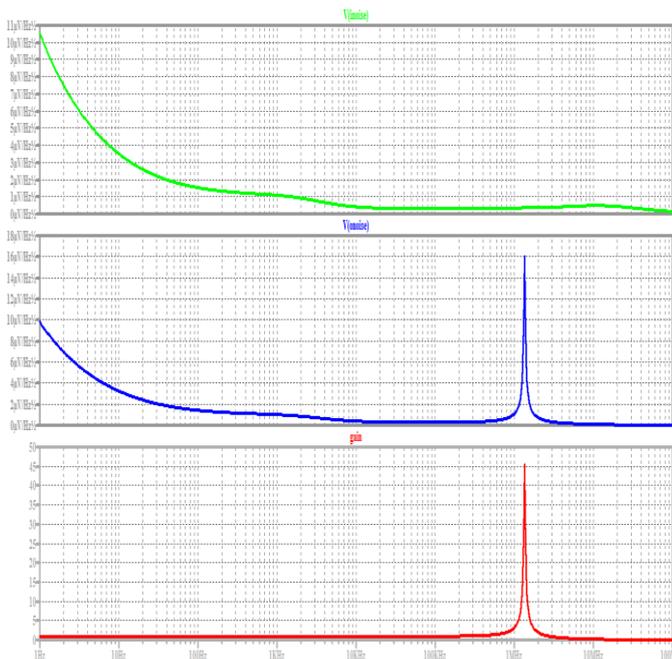


Figure 13 Noise Analysis for Amplifier

6. CONCLUSION

The study of Data converter design and designing approach of first order and second order data converters using single bit ADC and DACs is done. Performance using behavioral simulations using nearly ideal components to determine fundamental performance limitations using suitable Data converters topologies. Use of SCMOS VLSI design and simulate the operation of data converters in stages is also studied and analyzed. Keeping in mind the above study an outline to design and analyze the data converters is being sketched. The designed data converters will be analyzed for high order frequencies namely MHz to THz.

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