International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 06 | June-2016 www.irjet.net p-ISSN: 2395-0072

Design of 64-bit hybrid carry select adder using CMOS 32nm Technology

Gurdeep Kaur[1], Candy Goyal[2], Kuldeep Singh[3]

[1] M.Tech Student, Yadwindra College of Engineering, Talwandi Sabo, India
[2]Assistant Professor, E.C.E Deptt. of Yadwindra College of Engineering, Talwandi Sabo, India
[3] Lecturer, E.C.E Department of Guru Ram Dass Institute of Engineering and Technology, Bathinda, India
[1]gurdeepnoor@gmail.com,[2]engg_candy@gmail.com,[3]kuldeep649@gmail.com

---

Abstract - *This paper presents low leakage carry select adder (CSA). CSA is one of the fastest adders used in many data-processing systems to perform fast arithmetic operations. In this paper Carry Select Adder uses single RCA and binary to excess-1 converter (BEC) are used instead of dual RCAs to optimize average and leakage power dissipation. The reason for leakage power reduction is that, the number of logic gates used to design a BEC is less than the number of logic gates used for a RCA design. Thus, importance of BEC logic comes from the large silicon area reduction when designing CSA for large number of bits. 64-bit CSA adder using hybrid architecture is analyzed in this paper. The circuit design is simulated at 32nm Technology using Tanner EDA v(13.0). Results shows that 64bit CSA has better performance parameter as compared to the conventional CSA*.

Key Words: **Conventional carry select adder (CSA), Binary to excess-1 converter (BEC), Ripple carry adder (RCA)**

1.INTRODUCTION *(Size 11 , cambria font)*

Performance of modern digital system is dependent on the performance of individual circuits that form various functional units. Adders are one of the widely used block in digital integrated circuits. High speed adder is the necessary component in a data path of microprocessors and a DSP processor. Among the performance parameter, leakage power is critical as the technology improves. Because of threshold voltage reduction leakage current increases exponentially with the gate source voltage [1].As adder is critical part of almost all the modern digital system.Optimization of leakage power in adder can optimize overall leakage power of the circuits. In this paper two 64bit carry select adder with hybrid adder is designed and analyzed. We have used 10T and 14T full [11] adder because these two adders is having lesser leakage power as compared to the other design styles presented in the literature. The simple type of parallel adder is a ripple carry adder, which uses a chain of one bit full adder to generate its output. The Ripple Carry Adder (RCA) [1] gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but lead to increase in area. The Carry Select Adder (CSA) provides a compromise between small area but longer delay than Ripple Carry Adder (RCA) and having larger area with shorter delay than Carry Look-Ahead Adder (CLA) [1].Hybrid adder architecture is improved in terms of performance parameters. For the global carry generation in hybrid adder, a simple parallel scheme is used to relieve the fan-out load at the final multiplexer stage. The parallelism does not require intermediate outputs in the carry select scheme in hybrid architecture. In hybrid adder, internal carry generation logic is shared to minimize area of adder.

2. Review of Adder Architectures

To add multiple inputs various types of Adder Architecture are presented in literature which is explained as given below:-

2.1 Ripple Carry Adder (RCA)

Two binary words, each with n-bits, can be added using a ripple carry adder. Fig-1 shows the circuit for a 4-bit ripple carry adder. The carry input to the least significant bit is normally set to 0(c0), and the carry output of each full adder is connected to the carry input of the next most significant (MSB) of full adder [3]

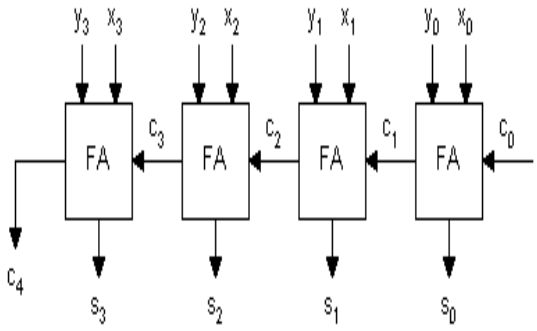

Fig: 1.Block diagram of RCA [8]

RCA design occupies the small area but takes longer computing time. The delay of RCA is linearly proportional to number of input bits.

2.2 Carry Look ahead adder (CLA)

Carry Look ahead adder speed up the operation of addition, because in this scheme carry for the next stages is calculated in advance, based on input signals .The CLA offers a way to eliminate the ripple effect in RCA.CLA is faster than RCA but consumes large area [4].

Pi = Xi XOR Yi --- Carry Propagation

Gi = Xi AND Yi --- Carry Generate

$S = P_i \oplus C_i$

Ci+1 = Gi or (Pi AND Ci)--Next Carry

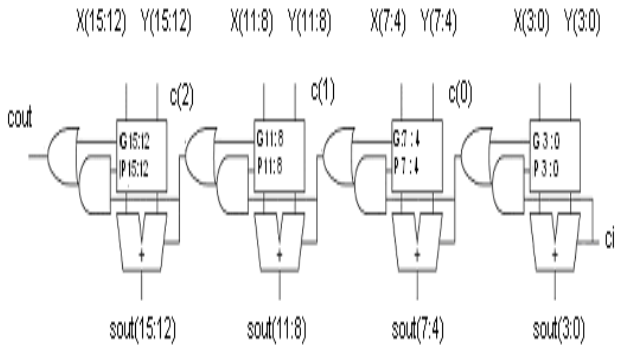

Fig:-2.Block diagram of 16-bit carry look ahead adder [4]

2.3 Carry Skip Adder (CSKA)

In case of N-bit Ripple carry adder, carry has to propagate through all N stages, which results in large delay in performing binary addition. In contrast, it is possible to skip carry over group of n-bits in case of Carry Skip Adder [4].Carry skip adder has large delay as compared to CLA but less than RCA.

Carry Propagate: Pi=Ai⊕Bi

Sum: Si=Pi⊕Ci

Carry Out: Ci+1= Ai Bi+ Pi Ci

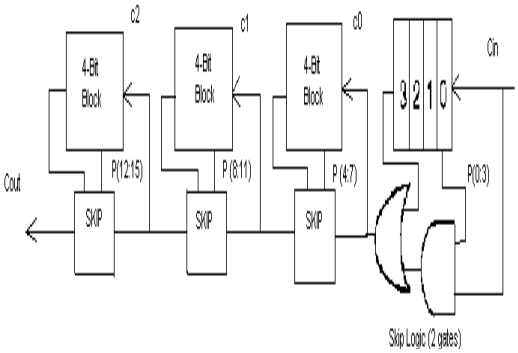

Fig:-3. 16-Bit Carry-Skip Adder [4]

2.4 Carry save adder

Basically, carry save adder is used to compute sum of three or more n-bit binary numbers. Carry save adder is same as a full adder [5].Boolean equations for sum and carry signals are given below:-
Si = Xi XOR Yi
Ci = Xi AND Yi

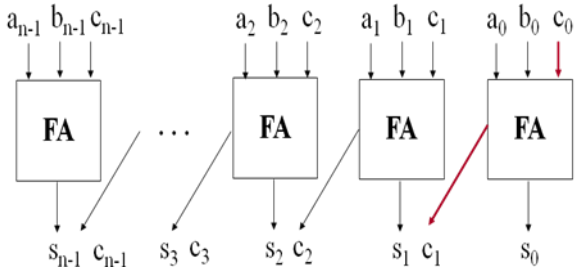

Fig:-4. N-bit Carry save adder [4]
Carry save adder reduces the leakage.

2.5 Conventional Carry Select Adder (CSA)

Carry select adder is based on the principle to calculate sum that is based on assuming input carry from previous stage. One of the adder calculates the sum assuming input carry '0' while the other calculates the sum assuming input carry '1'. Then, the actual carry triggers a multiplexer that selects the appropriate sum. Carry output of each block is given to next block as input carry [6].

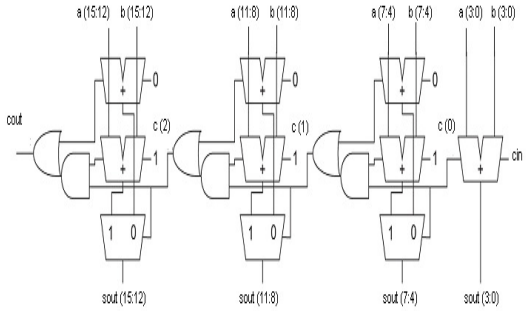

Fig:-5.Block diagram of 16-bit Carry select adder [4]

Performance of CSA adder is intermediate between longer delay of RCA and large area of CLA. But designing of CSA is more complex.

3. HYBRID CARRY SELECT ADDER

A Hybrid Carry Select-Adder is proposed. The modification is done by replacing lower 32bit LSB and upper 32bit MSB with different full adder circuits. In first architecture, 14T full adder is used for 32bit MSB and 10T full adder is used for 32bit LSB. In second architecture, 10T full adder is used for 32bit MSB and 14T full adder is used for 32bit LSB. Thus, importance of BEC logic comes from the large silicon area reduction when designing hybrid CSA for large number of bits. As to replace the N bit RCA, an N+1 bit BEC is used [1]. So in hybrid architecture of CSA, the 4-bit RCA is used in each block and thus the BEC used is of 5-bit wide. The MUX's are used to select either BEC output or the direct inputs according to the control singal.10 bit to 5 bit multiplexer are used to select the final output.

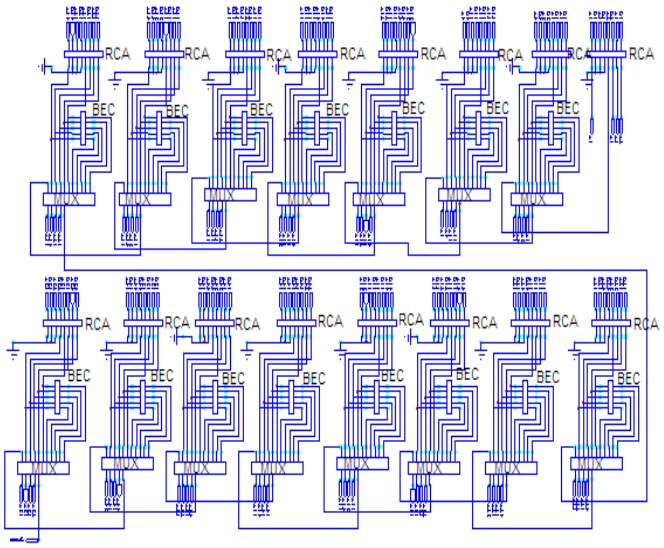

Fig: -6. Block diagram of 64-bit hybrid Carry select adder using (14T—10T)

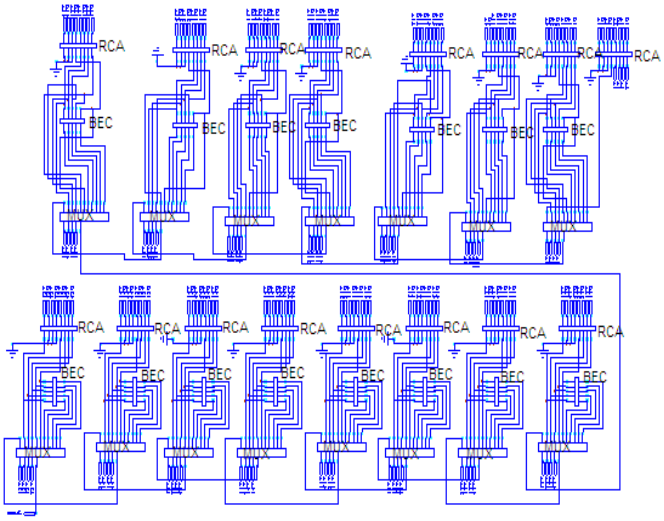

Fig: -7. Block diagram of 64-bit hybrid Carry select adder using (10T—14T)

SIMULATION RESULTS

Conventional carry select adder and Modified carry select adder using different types of adders are simulated using TANNER EDA v (13.0). All the simulations are performed at 32nm CMOS technology. 64-bit Conventional carry select adder has 1.77mw leakage power, 2.35mw average power consumption. The number of transistors of 64-bit conventional CSA is 3698.

TABLE 1: Leakage power, Average power consumption and number of gates of 1-bit full adders at 500MHz frequency.

Types of adders	Conv	10T	12T	14T	BV2
Leakage power (nw)	460	10	200	2	230
Average power (uw)	10.1	1.95	3.43	0.56	5.6
Number of transistor	28	10	12	14	24

TABLE 2: Leakage power, Average power consumption and number of gates of 64-bit hybrid carry select adders at 500MHz frequency.

Types of adders	64bit hybrid CSA using 10T(32bit MSB) and 14T(32bit LSB)	64bit hybrid CSA using 14T(32bit MSB) and 10T(32bit LSB)
Leakage power (mw)	0.44	0.47
Average power (mw)	0.74	0.72
Number of transistors	2120	2120

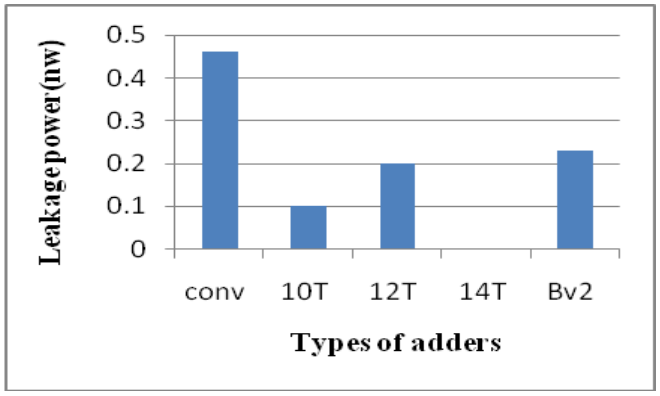

Fig:8.Comparison of Leakage power of 1-bit full adders

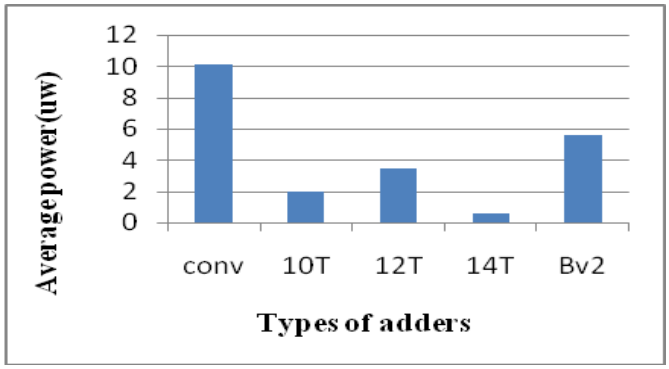

Fig:9.Comparison of average power comsumption of 1-bit full adders at 500Mhz frequency

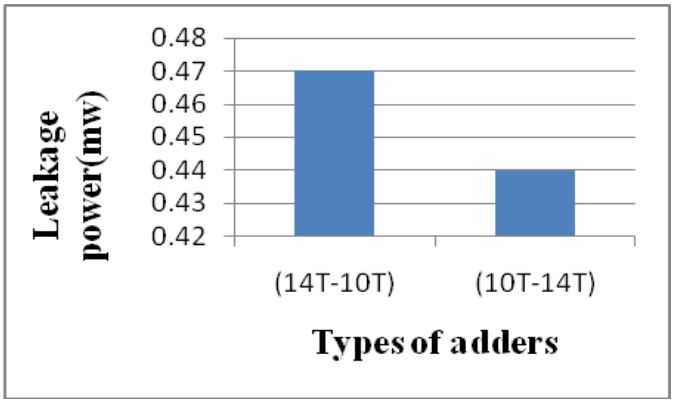

Fig:10.Comparison of Leakage power of 64-bit hybrid CSA using 14T and 10T adders

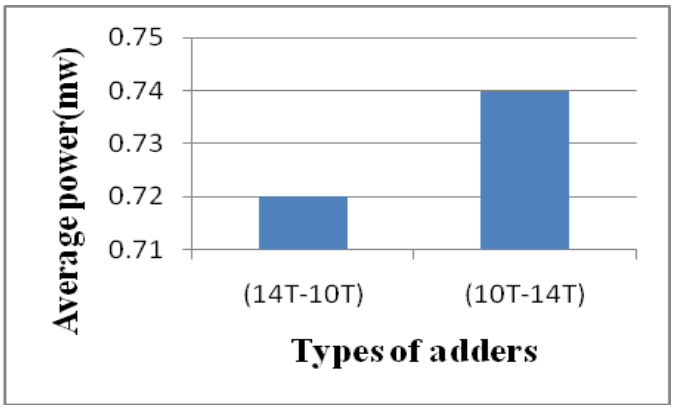

Fig:11.Comparison of average power consumption of 64-bit hybrid CSA using 14T and 10T adders at 500Mhz frequency

3. CONCLUSIONS

64-bit hybrid carry select adder shows better performance than conventional carry select adder. The basic idea behind of implementing various design units of carry select adder is to compare them with reference to the average power consumed leakage power. Simulation result shows the leakage power and average power of each carry select adder. From results it is concluded that 64bit hybrid CSA using 14T of a (32bit MSB) and 10T of a (32bit LSB) adder has better performance. The leakage power reduced 75% as compared to conventional carry select adder and average power 68% at 500MHz frequency.

REFERENCES

[1].Shivani Parmar,Kirat Pal Singh, "Design of high speed hybrid carry select adder", Advanced Computing Conference

(IACC), IEEE 3rdinternational,pp:165 1663,2013. 294, Dec. 2001, pp. 2127-2130, doi:10.1126/science.1065467.

[2].Ohsang Kwon, Earl E. Swartzlander, Kevin Nowka, "A Fast Hybrid Carry-Look ahead/Carry-Select Adder Design",IEEE International Symposium on Circuits andSystems,2006.

[3].Mohammad Reza Bagheri,"Ultra Low Power Sub-threshold Bridge Style Adder in Nanometer Technologies," Canadian Journal on Electrical and Electronics Engineering, Vol. 2, No. 7, 2011.

[4].R.P.P.Singh,Parveen Kumar, Balwinder Singh, "Performance Analysis Of Fast Adders Using VHDL"International Conference on Advances in Recent Technologies in Communication and Computing,pp-189-193,2009.

[5].B.Ram kumar, Harish M Kittur, P.Mahesh Kannan, "ASIC Implementation of Modified Faster Carry Save Adder", European Journal of Scientific Research ISSN 1450-216X Vol.42 ,No.1 , pp.53-58,2010.

[6].T.RantaMala,R.VijayKumar,T.ChandraKala, "Design and Varification of Area Efficient High-Speed carry select adder", International Journal of Research in Computer and Communcition technology (IJRCCT), ISSN 2278-5841,Vol. 1,Issue6,2012.

[7].Vaibhav Gupta, Debabrata Mohapatra, Anand Raghunathan,Kaushik Roy, "Low power digital signal processing using approximate adders",IEEE Transactions on computer Aided design of integrated circuits and systems,Vol.32,2013

[8]. D. Garg and M. K. Rai, "CMOS Based 1-Bit Full Adder Cell for Low-Power Delay Product", IJECCT, Vol. 2 (4), 2012.

[9].Padma Devi, Ashima Girdher, Balwinder Singh,"Improved Carry Select adder with Reduced Area and Low Power Consumption ", International Journal of Computer Applications, Vol.3, No.4, 2010.

[10].K.Saranya, "Low Power and Area-Efficient Carry Select Adder", International Journal of Soft Computing and Engineering
(IJSCE), ISSN: 2231-2307, Vol-2, Issue-6, 2013.

[11].Arvind Kumar, Anil Kumar Goyal, "Study of Various Full Adders using Tanner EDA Tool", International Journal of Science Technology (IJCST) Vol. 3, Issue 1, 2012.

[12].Saradindu Panda, A.Banerjee, B.Maji, Dr.A.K.Mukhopadhyay, "Power and Delay Comparison in between Different types of Full Adder Circuits",International Journalof Advanced Research in Electrical, Electronics and Instrumentation Engineering,Vol. 1, Issue 3, 2012.

[13].Subodh Wairya, Rajendra Kumar Nagaria, Sudarshan Tiwari,"Comparative Performance Analysis of XOR-XNOR function Based High Speed CMOS Full Adder Circuits For Low Voltage VLSI Design",(VLSICS)Vol.3,No.2.2012.

[14]. N.Weste,A.Eshragian,"Principal of CMOS VLSI:system perceptive", Pearson/ Addision Wesley publisher,2005

[15]. Jun Cheol Park , Vincent J. Mooney, "Sleepy Stack Leakage Reduction", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 14, No. 11, 2006.