

# AREA EFFICIENT ROUTER ARCHITECTURE DESIGN OF NETWORK-ON-CHIP(NOC)

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**Abstract** - In this project work we introduce a high performance and power efficient reconfigurable Network on Chip applications router. The designed reconfigurable router as compared to other router consumes less power and has high performance. The power gating technique is used which causes less power dissipation of this reconfigurable router. And with the help of xpower analyser total area is calculated. This router has four channels (namely, east, west, north and south) and a crossbar switch. Each channel has First in First out (FIFO) buffers and multiplexers. to store the data FIFO buffer is used and to control the input and output of the data Multiplexer is used. In the present work for router design entry we used Verilog Hardware Description Language. XILINX ISE Design Suite 14.7 are used for simulation and synthesis respectively. South channel is designed first which included the design of FIFO and multiplexers. After that, the crossbar switch and other three channels are designed. All these designed channels, FIFO buffers, multiplexers and crossbar switches are combinably to form the complete structure of this router architecture. By using Xilinx ISE tool RTL viewed is obtained this proposed router architecture is simulated using Modelsim. The proposed reconfigurable router is synthesized using Xilinx SPARTAN-6 FPGAs.

**Key Words:** Fifo, Vhdl, Noc, Router, FPGA.

## 1. INTRODUCTION

The first idea of IC was given by Jack Kilby in 1958. An Integrated Circuit (IC) is integration of one or more gates designed on a single silicon chip and according to Moore's law transistor density will become double every 18 months. Latest IC made of thousands or millions of micro electronic device. These are designed and electrically related on silicon chip. Generally usage integrated circuit has also belongs to monolithic integrated circuits. The physical dimension of CMOS transistors on an integrated circuits are expected to cross the 10 nm threshold[1]. Memory circuits are highly regular, and thus more no. of cells

can be integrated with much less area for interconnects. This is the dominant reasons why the rate of increase of chip complexity (transistor count per chip) is regularly increases for memory circuits[2]. Network on Chips concept have been introduced to integrate several Intellectual Property (IP) cores results in high communication bandwidth and prallesim[3].

## 2. LITERATURE SURVEY

The advantage of the use of an NoC with reconfigurable routers as compared to homogeneous router. by reconfiguration, the buffer depth of each channel can be dynamically changed, according to the requirement of the application, thereby increasing the power efficiency of the system for the same performance level. We verified that to reach the same performance obtained with the reconfigurable router, the original architecture requires more buffers. given by Débora Matos, Caroline Concatto, Márcio Kreutz, Fernanda Kastensmidt, Luigi Carro, Altamiro Susin. A novel adaptive routing algorithm for spidergon NoC given by. [1] Rimpay Bishnoi, Pankaj Kumar, Vijay Laxmi, Manoj Singh Gaur, Apoorva Sikka, the nature of this routing scheme is minimal, adaptive and distributed. It proposed the current network traffic status and distributes traffic across all links evenly by taking advantage of path diversity available in spidergon. They used 2 virtual channels and modified standard router of spidergon architecture by adding support for each virtual channel at each input port to fully exploit the potential of our scheme to overcome deadlock problem. The exigency for heterogeneous many-core systems has brought an exponential growth in the complexity of their interconnections[2]. Debora Matos, Marcio Kreutz, Cezar Reinbrecht, Luigi Carro, Altamiro Susin, By this, other Network-on-Chip (NoC) alternatives are being sought to attend the requirements in terms of performance and power

consumption. Even though, some of these proposals represent very complex architectures, with virtual channels, tables and extra controls. Due to the use of minimum cost components in this structure, power and performance are improved. The proposed junction of two advantageous techniques: hierarchical topology with adaptability. The use of these two schemes is novel in the literature and it allows ensuring high performance even when the application has their communication rates altered. Rapid increase in the number of processor cores on a chip proposed by [3] Edward Kresch and Xiaofang Wang, packet-switching networks on chip (NoCs) have emerged as a promising paradigm for designing scalable communication infrastructures for future multi-core processors. The quest for high-performance networks, however, has led to very area-consuming and complex routers with marginal return in performance. Besides that, studies show that at the cost of power consuming and expensive buffers real parallel applications generate traffic at a much lower rate than the offered rate. With a 19-node network show that our network, in addition to its lower cost, gives low network latency under low to medium network load, which matches the communication needs proposed by applications for multicore processors provides extensive simulation results. This work represents a low-cost with only a buffer in each router in our hexagonal network design. Efficient routing algorithms are introduced. Network-on-Chips (NoCs) are replacing conventional buses as the interprocessor communication architecture by, [4] Chin Hau Hoo and Akash Kumar. There is a requirement of dynamic reconfigurable network on chip, since different use cases might be running on MPSoCs. But most dynamically reconfigurable NoCs because of addition logic of reconfiguration having large area overhead. Other dynamic reconfiguration, NoCs which are based on partial reconfiguration have high reconfiguration delay and needs off-line bitstream generation for all possible situations.

### 3. PROPOSED WORK

#### A. NOC ROUTER ARCHITECTURE

This router design gives network on chip mesh network with dynamic arrangement of the modules in network. Every message coming to each port is first stored in input buffer then this routing logic and control unit it determines the next path or destination path. The design shows that input port and output port separated for each port. According to the direction

message is passed to appropriate output line. The router switch in Fig consists of five ports namely north, south, east, west and local port. Router define- This NoC router is designed to be works on the following coding shows below:

- In this routing we have 4 I/P and 4 O/P routing coding.
- There are the two input and the one output in FIFO.
- There are 4 input and the input is the 8-bit data in crossbar.
- The crossbar represents the signal.
- The component of crossbar switch and component of FIFO are present in the router.

#### B. CROSSBAR

This crossbar consists of different components which contributes to provide the path to data. For example: arbiter, Control Unit, Encoder, 4x1 multiplexer. Crossbar is the dominant part of the Network on Chip architecture. The important function of the crossbar is to give the path to the data, as shown in fig below.

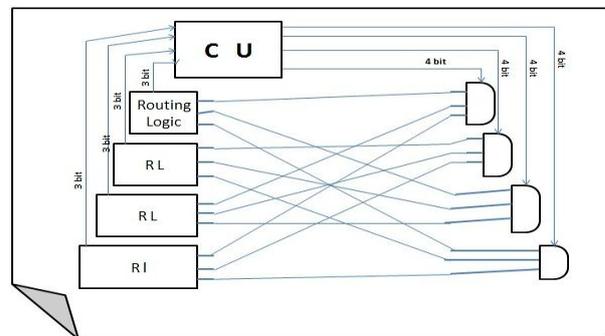


FIG1: CROSSBAR

Crossbar is define in coding language:

- 5X1 multiplexer is used in this design.
- We are using 5 I/P and the O/P in the crossbar coding.
- We used 1 I/P and 2 O/P in FSM.
- 3 I/P and the 1 buffer with round robin are used in the crossbar.
- In this coding the components are arranged in the fsm, round robin, encoder and the control unit.
- Design 4 has I/P and the O/P are used them in control

unit signal are define on them.

-1 I/P and the 1 O/P are used in the encoder .

**EAST PORT** : -The east port is used as a channel in the router.

-In the east port there are 3 I/P and 2 O/P works

-The FIFO component are work on FIFO.

-the FIFO component have 2 I/P and the 2 O/P.

### C.ENCODER

We used 4 I/P and 1 O/P encoder in this work.in this encoder at any point of time only 1 I/P port at the crossbar can drive 1 O/P port.The encoder produces select signal for each O/P port when signals from arbiter block and using output address receives by encoder which is stored in state machine.

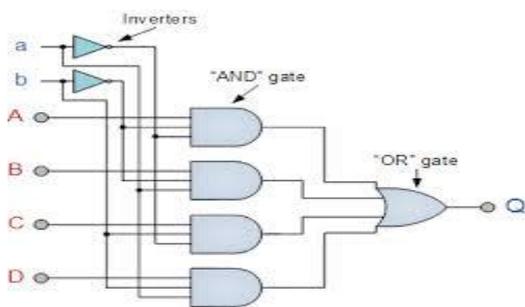


FIG2. ENCODER 4X1

### SIMULATION & ANALYSIS REPORT

#### 1.Multiplexer 4X1

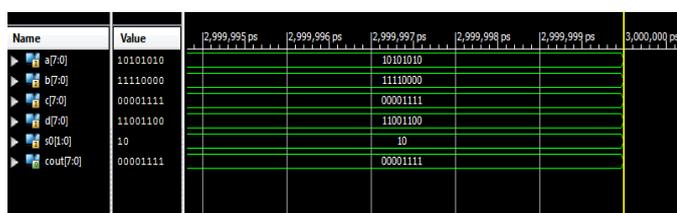


Figure-3

Synthesize report shows the Delay of 2.796ns. And the power consumption is 6.89mw.

#### 2.Control Unit

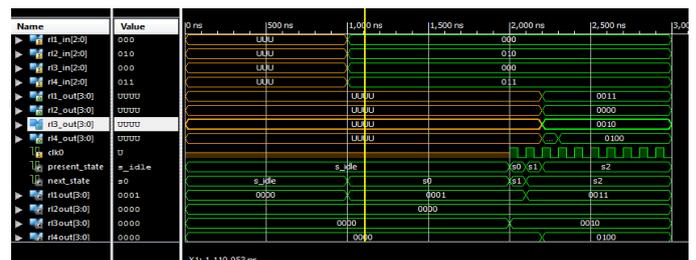


Figure-4

#### 3.East Port

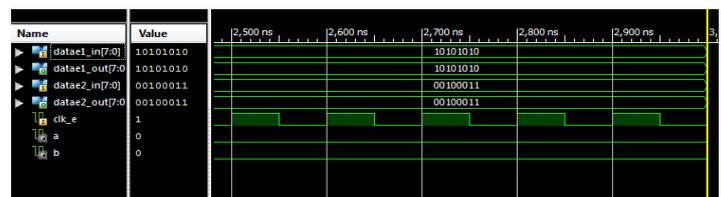


Figure-5

Synthesize report shows the Delay of 1.66ns. And the power consumption is 1.02mw.

#### 4.Crossbar.



Figure-6

#### 5.Noc Router

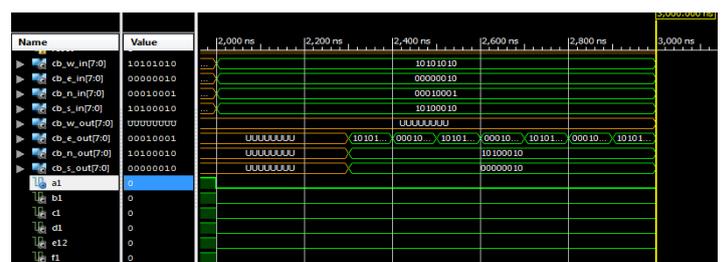


Figure-7

Synthesize report shows the Delay of **2.796ns**. And the power consumption is **6.89mw**. Delay on the simulation of the circuit is **2.796ns**.

**Table1:Comparison in area consumption in each module**

Power	Lut	Delay	Lut(comparison)
<b>Original router</b>	<b>Original router</b>	<b>Original router</b>	<b>Proposed router</b>
<b>6.893</b>	<b>163</b>	<b>2.796</b>	<b>235</b>

### 3. CONCLUSIONS

In this router architecture with simple decoding logic with all well working components total time taken by architecture is 4ns only which shows a good response speed. The characteristics of 5 port router design for NoCs with great performance and its routing algorithm can be understood very well by simulation. This architecture providing with right i/p performs very well in XILINX ISE 14.7. The synthesis and simulation of the proposed router is verified by using Xilinx ise software with VHDL code.

#### REFERENCES

- [1]Débora Matos, Caroline Concatto, Márcio Kreutz, Fernanda Kastensmidt, Luigi Carro, Altamiro “Reconfigurable Routers for Low Power and High Performance”
- [2]Rimpy Bishnoi, Pankaj Kumar, Vijay Laxmi, Manoj Singh Gaur, Apoorva Sikka “Distributed Adaptive Routing for Spidergon NoC”
- [3]Mrs. S. Ellammal M.E1, T.Saranya2 “Transparent Test Scheme in Online BIST For Word-Oriented Memories”
- [4]M.H. Husin, S.Y. Leong, M.F.M. Sabri, R. Nordiana “Built in selftest for RAM Using VHDL”