

Realization of a high speed RF data acquisition system

Yashaswini DJ¹, Muniraju², Nayana DK³

PG Student, Mtech in VLSI Design and Embedded systems, REVA ITM Bangalore- 560064¹ Design Engineer - Centum Electronics Limited,Bangalore² Asst. Prof. , (ECE), REVA ITM,Bangalore³

Abstract—This is an era of ELECTRONIC WARFARE. The modern technologies used to exploit the *Electromagnetic Spectrum are remarkable. Hence this paper* presents the design and implementation of a high speed RF Data acquisition system which will characterize an RF signal by extracting the primitive parameters like Frequency and Phase. Characterization of RF signals is very important in ELINT systems as the parameters of the RF signal through a RADAR will help in determining the exact location and source of the RADAR. The Data Acquisition System is a part of the QDR (Quad Digital Receiver). The algorithms of the sub modules which constitute the Data Acquisition System are implemented in VHDL. The synthesis and simulation results have also been presented.

Key words—Electronic warfare; Quad Digital Receiver; Data Acquisition; RF Data;

1.INTRODUCTION

In Electronic Warfare it is very essential to accurately determine the radar's intrapulse parameters in real time, so that the radar signal can be characterized accurately. This characterization plays a very important role as it aids in estimating the possible counter action against the intended radar. Primary focus would be to determine the fundamental parameters like frequency, amplitude, direction and time of arrival and pulse width of the radar signals. Though Analog receivers have the capability to measure the fundamental parameters they have a limitation towards sensitivity and accuracy. Hence digital receivers have made a fine mark in such systems by overcoming the limitations.

2. OVERVIEW QDR SYSTEM

2.1 Description

The Quad Digital Receiver (QDR) is an important subsystem of the satellite based ELINT payload for determining intrapulse parameters such as instantaneous frequency, amplitude, direction of arrival, pulse width of the radar signals in real time.

2.2 Functionality of a QDR system

It detects the video threshold in order to aid data acquisition. It also measures the signal frequency using Digital Instantaneous Frequency Measurement (DIFM) technique. It aids in measuring various parameters such as amplitude, pulse width using the analogue video signal. It computes the angle of arrival (AOA) using the Base Line Interferometry technique by simultaneously sampling the four IF signals corresponding to four antenna elements of the Azimuth/Elevation array.

2.3 Operation

The QDR accepts an IF channel in the frequency range of 1000 ± 250 MHz/ 160 ± 20 MHz for Instantaneous Frequency Measurement and two Video channels for signal detection/threshold and pulse parameters estimation are also available at the input of QDR.

It also accepts 4 channels for direction finding applications. The IF signals are amplified in signal conditioning circuits and passed through 3dB Hybrid to generate I and Q signals, which are digitized using high speed ADC's. The logic in FPGA receives the digitized signals with which it determines phase, frequency and angle of arrival of the signal. The video channel is used to generate the data valid trigger and this enables the measurement of pulse width. The output from the receiver is packetized as PDW (Pulse Description Word) and transmitted to data handling system.

3.DATA ACQUISITION SYSTEM

This paper presents the design and implementation of one of the modules in QDR system which determines the Phase and Frequency. Fig. 1. depicts the block diagram high speed data acquisition with ADC at 625MHz for frequency measurement. The IF channel is first passed through a signal conditioning circuit and then through high speed ADCs (Analog-to-Digital converter) and then the signal is given to the logic in the FPGA. In addition to that two video channels are given for threshold detection

3.1 System Description

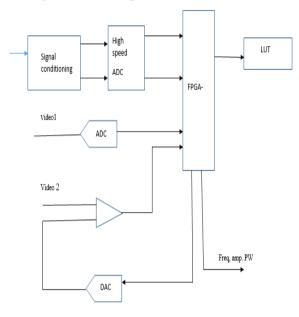


Fig. 1.Data Acquisition system showing the inputs and outputs $% \left[{{\left[{{{\mathbf{F}}_{i}} \right]}_{i}}} \right]$

The output is the phase and frequency. With some additional circuitry and logic, it is also possible to determine the amplitude and pulse width. An external LUT (Look Up Table) is present in order to calculate the frequency with the help of the phase obtained as an output from FPGA.

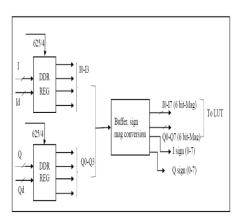


Fig. 2. Process flow of the Data Acquisition System

3.2 Basic Operation

Fig. 2. represents the process flow of the system. The first step is data acquisition in the DDR register. The instantaneous frequency measurement is carried out in this FPGA by using DDIFM technique.

Once the data is obtained, it is given as read address to the LUT. Look up tables are constructed using the block RAMs. From the available data, phase computation is done and the phases are pipelined into 128 phases. 128 samples are acquired and processed for getting the frequency update. Threshold is generated by an external high speed comparator. The reference for the comparator is generated by DAC whose input is programmable within FPGA. The FPGA is connected to the controller via SPI bus. The processor at power ON initializes the phase angle LUT and external LUT for frequency measurement. Data I and O (MSB 6+1 bits) is acquired in DDR mode by FPGA-1 at 625/4 MHz The 8 samples of I and Q are arranged as a block, for processing. The most likely phase is obtained through normalization and then the frequency is computed using the external Look up table.

The modal filtering concept is used for removing the invalid samples for getting better estimate of the frequency.

Data I and Q (MSB 6+1 bits) is acquired in DDR mode by FPGA-1 at 625/4 MHz The 8 samples of I and Q are arranged as a block, for processing.

3.3 LUT Configuration

 $4K \times 1$, 7 RAM blocks are used as LUT for getting phase directly from I and Q inputs. 8 such sets are instantiated for getting 8 phases simultaneously at (625/8) MHz (\approx 12.8nsec). Block RAM read out time with 8 fan outs \approx 8nsec.

7 RAM blocks (4K×1) are concatenated for (4K×7). The LUT Data (0 to 900) is loaded by CPU. The output is read using magnitude I&Q as address. The sign bit of I and Q with LUT output is used in generating 0-359 phase output

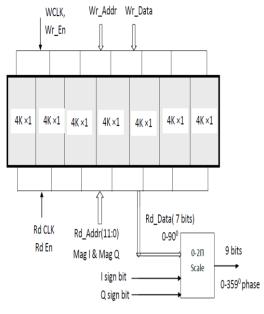


Fig. 3.BRAM configuration

3.4 Modal filter and Phase measurement

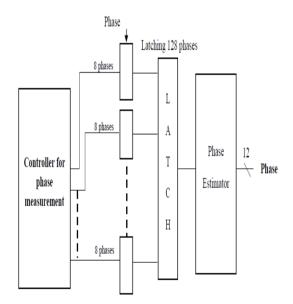


Fig. 4. Phase Measurement

The difference between adjacent phases will be computed with added delay of 2π . These difference phases will be sorted into 16 groups and the group with the maximum concentration will be used. The mean value of the phase in the most concentrated group is assumed as best estimation. 3 such filtering will be employed to get difference phases ϕT , $\phi 4Ts$ and $\phi 16Ts$. These phases are

input to the ambiguity resolving logic module and the module outputs the unwrapped phase $\varphi 16 Ts.$

3.5 Phase to Frequency

The unwrapped phase output ϕ 16Ts addresses the external memory LUT where frequency values are stored. One Frequency output is generated for every 128 input samples which is used for phase correction and direction finding in other FPGAs.

4.SYNTHESIS AND SIMULATION RESULTS

4.1 Data acquisition through DDR

Fig. 3. shows the data acquisition result through the DDR. The data passed through four DDR registers will result in 8 data. Hence four component of I and Q data each gives a total of sixteen output data lines.

4.2 BRAM Configuration

The LUT is constructed by cascading 7 block RAMs in each set and a total of eight such sets are configured. This implies that a total of 56 block RAMs are used to configure the LUT.

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<u>- 1-</u>		Msgs																
•	/data_acq_tb/data_in1_p	199	24	25	26	27	28	29	130	31	32	33	34	35	36	37	38	39
	/data_acq_tb/data_in2_p	142	48	50	52	54	56	58	60	62	64	66	68	70	72	74	76	78
•	/data_acq_tb/data_in3_p	85	72	75	78	81	84	87	90	93	96	99	102	105	108	1111	114	117
•	/data_acq_tb/data_in4_p	28	96	100	104	108	112	116	120	124	128	132	136	140	144	148	152	156
	/data_acq_tb/data_in1_n	56	231	230	229	228	227	226	225	224	223	222	221	220	219	218	217	216
•	/data_acq_tb/data_in2_n	113	207	205	203	201	1199	197	195	193	191	189	187	185	183	181	179	177
•	/data_acq_tb/data_in3_n	170	183	180	177	174	171	168	165	162	159	156	153	150	147	144	141	138
•	/data_acq_tb/data_in4_n	227	159	155	151	147	143	139	165	131	127	123	119	115	1111	107	103	99
	/data_acq_tb/data_out_i_0_tb	195	21	23		25		27		29		31		33		35		37
• • •	/data_acq_tb/data_out_j_1_tb	196	22		24		26		28		30		32		34		36	
• •	/data_acq_tb/data_out_i_2_tb	196	22	24		26		28		30		32		34		36		38
•	/data_acq_tb/data_out_i_3_tb	197	23		25		27		29		31		33		35		37	
•	/data_acq_tb/data_out_i_4_tb	134	42	46		50		54		58		62		66		70		74
🔳 ┥	/data_acq_tb/data_out_j_5_tb	136	44		48		52		56		60		64		68		72	
• •	/data_acq_tb/data_out_i_6_tb	136	44	48		52		56		60		64		68		72		76
•	/data_acq_tb/data_out_i_7_tb	138	46		50		54		58		62		66		70		74	
• •	/data_acq_tb/data_out_q_0_tb	76	66	72		78		84		90		96		102		108		114
🔳 ┥	/data_acq_tb/data_out_q_1_tb	79	69		75		81		87		93		99		105		111	
•	/data_acq_tb/data_out_q_2_tb	73	63	69		75		81		87		93		99		105		(111
•	/data_acq_tb/data_out_q_3_tb	76	66		72		78		84		90		96		102		108	
• •	/data_acq_tb/data_out_q_4_tb	16	88	96		104		1112		120		128		136		144		152
🔳 ┥	/data_acq_tb/data_out_q_5_tb	20	92		100		108		116		124		132		140		148	
•	/data_acq_tb/data_out_q_6_tb	12	84	92		100		108		116		124		132		140		148
•	/data_acq_tb/data_out_q_7_tb	16	88		96		(104		1112		(120		128		136		144	کھ
	/data_acq_tb/sysck_p	1																
	/data_acq_tb/sysck_n	0																کا کا ت

Fig. 5. Process flow of the Data Acquisition System

₩	Msgs																		
🔷 /bram7_cas_tb/dk_tb	1																		
	14	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
	14	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
	4	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	4	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
🕀 🔶 /bram7_cas_tb/read_data_tb	1				0		1	2	3	4	5	6	7	8	9	10	11	12	
	0	0																	
₽-� /bram7_cas_tb/q_data_in_tb	3	0			1	2	3	4	5	6	7	8	9	10	11	12	13	14	
₽-♦ /bram7_cas_tb/r_data_in_tb	0	0																	
₽→ /bram7_cas_tb/s_data_in_tb	14	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
/bram7_cas_tb/write_en_tb	1																		
🔶 /bram7_cas_tb/read_en_tb	1																		
🔶 /bram7_cas_tb/rst_tb	1																		
	14	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
📕 🄶 /bram7_cas_tb/write_addr_tb	14	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Fig. 6. BRAM Configuration

-	Misgs																	
	137	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
+ /normalize_tb/data_2_tb	273	221	223	225	227	229	231	233	235	237	239	241	243	245	247	249	251	253
	409	331	334	337	340	343	346	349	352	355	358	361	364	367	370	373	376	379
🗉 🔷 /normalize_tb/data_4_tb	33	[441	1445	1449	453	457	461	465	469	473	477	481	485	(489	493	497	501	1505 19
🗉 🔷 /normalize_tb/data_5_tb	169	39	44	49	54	59	64	69	74	79	84	89	94	99	104	109	114	119
+ /normalize_tb/data_6_tb	305	149	155	161	167	173	179	185	191	197	203	209	215	221	227	233	239	245
+ /normalize_tb/data_7_tb	441	259	266	273	280	287	294	301	308	315	322	329	336	343	350	357	364	371
	65	369	377	385	393	401	409	417	425	433	441	449	457	465	473	481	489	497 1
	137	1111	1112	1113	1114	1115	116	1117	1118	119	1120	121	122	123	124	1125	126	127
	274	222	224	226	228	230	232	234	236	238	240	242	244	246	248	250	252	254
+ /normalize_tb/counter3_tb	411	333	336	339	342	345	348	351	354	357	360	363	366	369	372	375	378	381
+ /normalize_tb/counter4_tb	36	444	448	452	456	460	464	468	472	476	480	484	488	492	496	500	504	508 0
	173	43	48	153	58	63	68	173	78	83	38	93	98	103	1108	1113	1118	123 1
	310	154	1160	1166	172	178	184	1190	196	202	208	214	220	226	232	238	244	250
	447	265	272	279	286	293	300	307	314	321	328	335	342	349	356	363	370	377
+ /normalize_tb/counter8_tb	72	376	384	392	400	408	416	424	432	440	448	456	464	472	480	488	496	504
+ /normalize_tb/data_res1_tb	495	469	470	471	472	473	474	475	476	477	478	479	480	481	482	1483	484	485
	495	469	470	471	472	473	474	475	476	477	478	-1479	1480	481	1482	483	484	(485)
🗉 🔷 /normalize_tb/data_res3_tb	343	469	470	471	472	473	474	475	476	477	478	479	-480	481	482	483	484	485
🗉 🔷 /normalize_tb/data_res4_tb	495	317	318	-619	-320	321	322	323	-324	325	326	327	328	329	330	331	332	333
	495	469	470	471	472	473	474	475	476	477	478	479	480	481	482	-483	484	485
+ /normalize_tb/data_res6_tb	495	469	-470	471	472	-473	474	475	476	477	478	-479	-480	481	482	483	-1484	485
🗈 🔷 /normalize_tb/data_res7_tb	343	469	-1470	471	472	473	474	475	476	477	478	479	4480	481	482	483	484	(485
🗉 🔷 /normalize_tb/data_res8_tb	438	468	461	454	-447	-1440	433	426	419	412	405	398	-1391	-384	377	370	363	356
/normalize_tb/clk_tb	1																	
A loormalize threat th	0																	

Fig. 7. Normalization

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P -	Msgs															
/phase_out_tb/clk_tb	1															
₽-<>> /phase_out_tb/p1_tb	1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
₽-� /phase_out_tb/p2_tb	2	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
₽-� /phase_out_tb/p3_tb	4	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
🖅 🔶 /phase_out_tb/p4_tb	3	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
💶 - 🎸 /phase_out_tb/p5_tb	5	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
💶	17	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
🖅 🕂 hase_out_tb/p7_tb	33	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
🗄 🔶 /phase_out_tb/pout_tb	4	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

Fig. 8. Phase output

5.CONCLUSION

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Different algorithms were implemented and the most optimized one was selected for the design. Optimization parameters considered were in terms of speed and resource utilization. Following the entire process flow, each sub module as designed as per the demanded specifications and the most likely phase was obtained considering a single slot. The frequency could be consequently calculated through the external LUT.

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