A survey on effective Automatic Test Pattern Generator for self-checking Scan - BIST VLSI circuits

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Abstract - This paper attempts to show the survey on ISCAS89 Sequential Benchmark circuits. Gate delay, propagation delay, no. of flip flops and total number of gates are listed and compared for benchmark circuits. The circuits were built in .asl file and simulated using AUSIM L2.3. Operating temperature, marginal supply voltage as well as an increased output load capacitance leads to variation in gate delay or in propagation delay. Depending on the circuit components placed one after another, the delay varies. All aspects are compared for the Benchmark circuits from s27 to s38584.

Key Words: Linear assembly, Test Pattern Generator, Linear Feedback Shift Register, Weighted and Transition Density Pattern

1. INTRODUCTION

The analysis of number of flip flops and total number of gates, gate delay and propagation delay for the benchmark circuits. The combinational connection of invertors, AND, NAND, OR, NOR in the benchmark circuits are compared. Comparison of all ISCAS89 benchmark circuits has least gate delay and propagation delay are 6 and 22, maximum of 127 and 1636 respectively.

2. DESIGN FOR TESTABILITY (DFT)

Design for testability is an IC design technique and adds testability feature for scheming hardware product. The added topographies make easier to develop and built-up tests to the proposed hardware. The purpose of built-up tests is to validate no manufacturing defects for the product and that could undesirably affect the product’s correct performance. The tests are generally propelled by impulsive test equipment that execute test programs.

3. SCAN-BIST

Scan chain is a method used in design for testing. The aim of the chain is to make testing easier by providing a simple way to set and observe every flip-flop in an Integrated Circuit. The basic structure of scan includes the following set of signals in order to control and observe the scan mechanism.

Scan-output and scan-in define the output and input of a scan chain. Each input drives only one chain and scan out observes one as well in a full scan mode. A scan enable pin is a special signal that is added to a design. When this signal is stressed, every flip-flop is connected into a long shift register.

During shift phase and the capture phase the clock signals are used guiding all flip flops in the chain. An arbitrary pattern can be inserted into the chain of flip-flops, and everystate of the flip-flop can be observed. In a full scan design, automatic test pattern generation (ATPG) is particularly simple.

Even a simple stuck-at fault requires a order of vectors for recognition in a sequential circuit. Also, due to the presence of memory elements, the controllability and observability of the internal signals in a sequential circuit in general much more problematic than those in a combinational logic circuit. These aspects make the difficulty of sequential ATPG much higher than that of combinational ATPG.

4. BENCHMARK CIRCUITS

It is primarily for testing. A benchmark is a point of reference by which something can be restrained. In surveying, a "bench mark" is a permanent mark established at a known elevation that is used as the basis for measuring the elevation of other topographical points. It is widely available, modern design to spur research on DFT.
5. PROPAGATION DELAY

When the input to a logic gate becomes stable and valid to change, to the time required for the output of that logic gate is stable and legal to change. Often on manufacturers’ datasheets this mentions to the time required for the output to stretch 50% of its final output level when the input variations to 50% of its final input level. To process data at a faster rate and improving overall performance by reducing gate delays in digital circuits that allows them. The determination of the propagation delay of a combined circuit requires to detecting the longest track of propagation delays from input to output and by adding each tp time along this track.

The difference in propagation delays of logic elements is the major contributor to glitches in asynchronous circuits as a result of race conditions. The principle of logical effort utilizes propagation delays to compare designs implementing the same logical statement.

Operating temperature, marginal voltagesupply as well as an increased output load capacitance leads to increase in Propagation delay. Propagation delay can be increased by the latter is the largest contributor. If the output of a logic gate is connected to a long trace or used to drive many other gates the propagation delay increases substantially.

Wires have an estimated propagation delay of 1 ns for every 6 inches (15 cm) of length. Logic gates can have propagation delays ranging from more than 10 ns down to the picosecond range.

It is a time related with any digital circuit and is the time between when an input to the circuit varies until that variation propagates through the circuit and changes the output. Every digital gate (And, Or, Inverter...) has its own propagation delay. For single gates this delay can be very short, maybe somewhere around nanoseconds or shorter. If the circuit grows larger and more components are placed one after another, the delay increases too.

6. GATE DELAY

The input of the logic gate changes its state to 0’s or 1’s. The output of the gate will probable to change its state as its result. The output will not change rapidly when the input changes. Instead, the output will change after a small delay. This delay is called gate delay. Ideally, this delay is a small as possible; typically, it is on the order of few nanoseconds or less. Often the delay, when the output changes from low or high is a different value than the delay when the output changes from high to low. It is non-zero-time amount of time to charge or discharge a capacitor in which the voltage cannot be changed instantaneously.

7. FAN-IN

After the minimization of circuit level and mapping to the primary gates (AND or OR) with infinite fan-in and fan-out. Minimum circuit Depth is 2 for all logic circuits in accordance to this definition. Because any logic functions can be expressed in sum of product form without any fan-in that limits all the product expressions can be executed by AND gates and summed by one OR gate.

The acute path includes in one AND gate and one OR gate, corresponds to circuit depth of 2. The assumption of infinite fan-in and fan-out are invalided. The dependence of the circuit is based on both gate fan-in and fan-out maximums.

When the maximum fan-in is 4 the the depth will be 2. When the maximum fan-in is decreased by 2, then the depth of the circuit will be increased by 4. The simulation results allow us to statistically qualify the tendency of the circuit depth versus limitation of fan-in for the multiple input and multiple output of the combinational logic circuits.

8. FAN-OUT

The current from the output is sufficient to charge the load gate(s’) input capacitor(s’) and wire capacitor within time. For OE circuits the maximum fan-out is limited by the ratio of the gate’s output. After minimizing the circuit might require large fan-out that is beyond the maximum fan-out limits to the existing gate.

Both methods cause circuits to increase in depth. To evaluate the circuit depth increase caused by limiting fan-out. A large gate fan-out is significant in succeeding a smaller circuit depth.

9. LOGIC GATES

A logic gate is a fundamental building block of a digital circuit. Most logic gates have two inputs and one output. Every terminal is in one of the two binary conditions low (0) or high (1), represented by unlike voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is about zero volts (0 V), while the high state is approximately five volts positive (+5 V).

10. TEST OPTIMIZATION TECHNIQUE

Test optimization will make a build potentially comprehensive a lot faster than a full build and test run. It should do this without substantially compromising the property of the feedback it gives; in other words, a quicker pass or fail result, but a reasonably precise pass or fail. There are two ways of ensuring a build completes quickly:

1. Run only the tests required to confirm the validity of the changes that triggered the build.
2. Run all the tests but in an optimal order: any failed tests from the previous build, all tests covering modified code, then in ascending order by test invocation time.
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CONCLUSION

According to the analysis the circuit has different gate delay and propagation delay. The gate delay affects the circuits by delay time effect of gates to produce the fanout of gates. The propagation delays emerge as the important time constraints for producing the output.

REFERENCES


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