Front end Design of shift registers using latches

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Abstract: This paper proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. This Proposed System Designed using Verilog HDL and Simulated through Modelsim 6.4 c and Synthesis by Xilinx tool.

I. INTRODUCTION

As we know that shift register are the basic building blocks in a VLSI circuit. Which are commonly used in many applications, such as digital filters, communication receivers and image processing ICs. Nowadays, as the size of the image data has continuously increasing due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. Process like image-extraction and vector generation VLSI chip uses a 4K-bit shift register. Hence word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

This paper proposes implementation of shift registers using pulsed latches, which makes use of a multiple non overlapping delayed pulsed clock signals instead of single pulsed clock signal.

II. OBJECTIVE AND TOOLS USED

Project Objective

The main objective of this project is design and implementation of shift registers using pulsed latches.
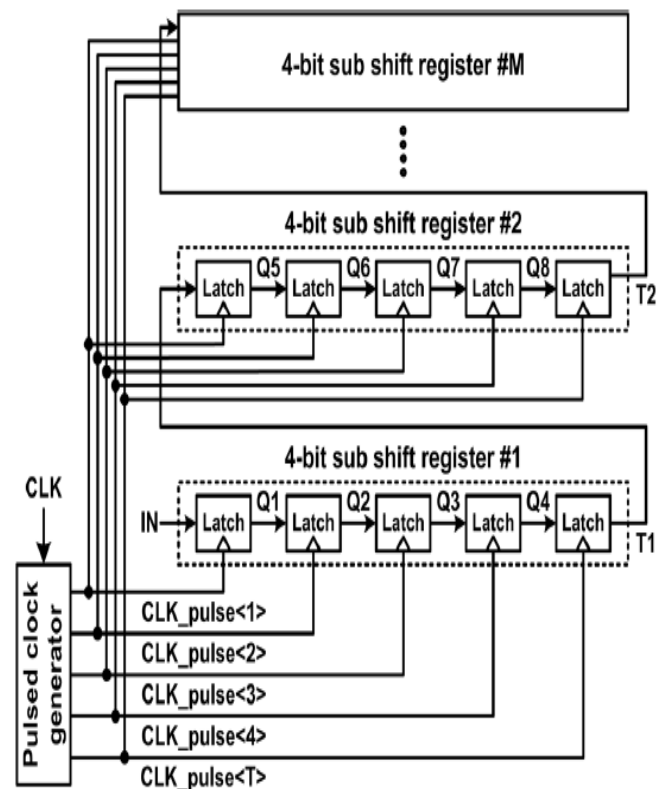
Simulation Software:

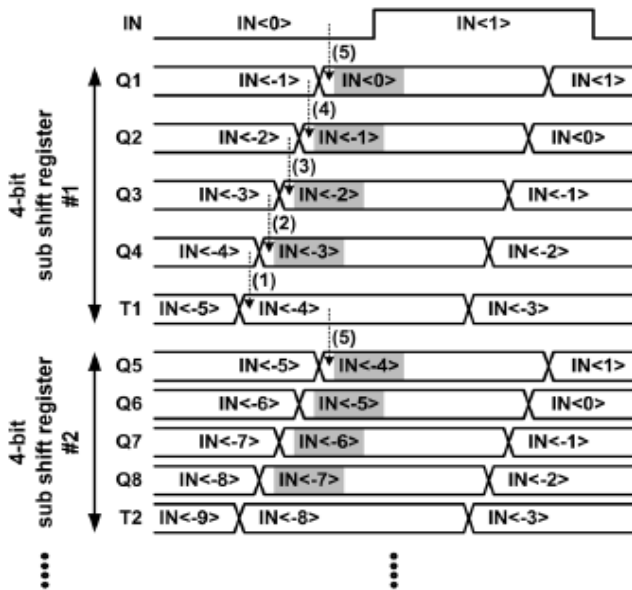Modelsim 6.4c is used for simulation of the proposed design.

Synthesis tool 9.1:

Xilinx 9.1 is used for synthesis of the design verilog code.

III. IMPLEMENATION

(a)

(b)

Fig1(a) proposed shift registers using pulse generator.(b)waveforms

Above fig1 (a) shows the proposed architecture design of shift registers using pulse latches. The proposed shift registers is divided into M sub shift registers to reduce the number of delayed clock signals. Here we use a 4 bit sub shift registers consisting of five latches and I performs shift operations with five non overlapping delayed pulse clock signals were sub shift register #1, four latches store 4bit data and last latch store tempoary 1-bit (T1) which will be stored and fed to next latch(Q5) of sub shift register#2 as shown in fig1(a) . fig1 (b) shows the operation waveform of the proposed shift registers. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 6. The sequence
of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal CLK_pulse<T> updates the latch data T1 from Q4. And then, the pulsed clock signals CLK_pulse<1:4> update the four latch data from Q4 to Q1 sequentially. The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.
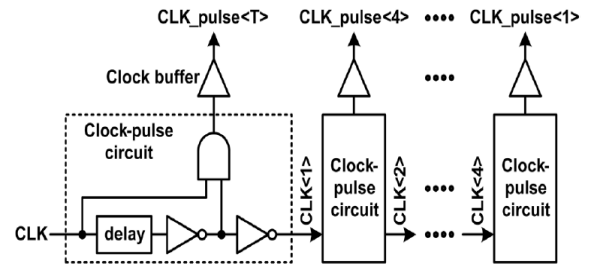

Fig2: delayed pulse clock generator circuit

The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in Fig. 2 each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an N-bit shift register is divided into k-bit sub shift registers, the number of clock-pulse circuits is K+1 and the number of latches is N+N/K. A K-bit sub shift register consisting of K+1 latch requires K+1 pulsed clock signals.

The number of sub shift registers (M) becomes (N/K), each sub shift register has a temporary storage latch. Therefore,(N/K) latches are added for the temporary storage latches. The conventional delayed pulsed clock circuits can be used to save the AND gates in the delayed pulsed clock generator in Fig. 2. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals. The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register (K). K is selected by considering the area, power consumption, speed.

IV.AREA AND POWER OPTIMIZATION

The area optimization is done through Xilinx9.1 and its results through normal flip-flops and using pulse latches are been compared and obtained results are shown below.
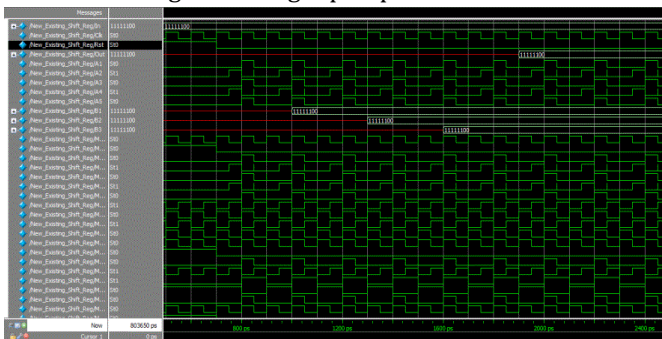
TABLE.1RESULTS

Type of shift register	No of bits	Area (gate count)	Power consumption(mv)
Using flipflops	4-bit	1368	39
	256-bit	20598	6511
Using latches	4-bit	862	38
	256-bit	12892	636

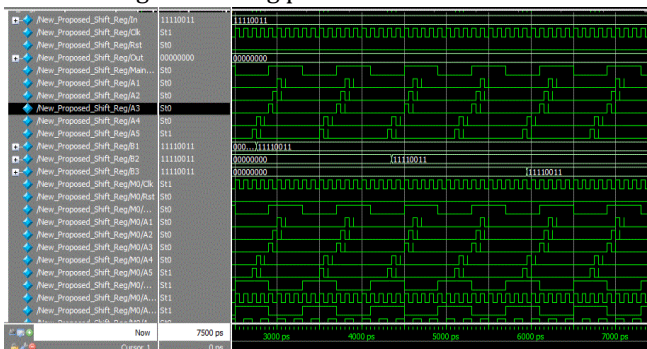The power analysis for the proposed method is done through Xpower analysis tool available in Xilinx.
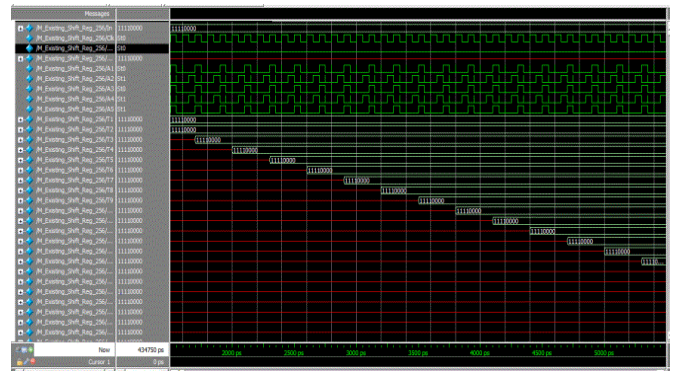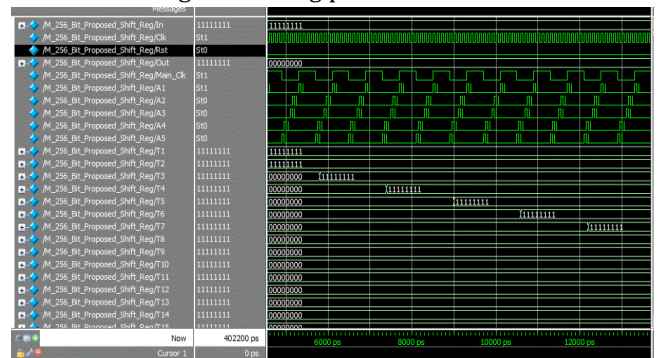
V. SIMULATION RESULTS

4-bit shift register using flip flops

4bit shift registers using pulsed latches

256 bit shift registers using flip flops

256 bit shift registers using pulsed latches

VI. CONCLUSION

The proposed paper is a low power and area efficient shift registers using pulsed latches. When by replacing flipflop with pulse latches power and area will be reduced. The timing problem between pulsed latches is solved using multiple non-overlapping delayed clock pulses. A verilog code is written for 4-bit and 256-bit shift registers and power and area analysis with respect to normal flip-flop and pulse latches is been carried on and desired results are obtained.

REFERENCES

[1]. S. Naffziger and G. Hammond, "The implementation of the next generation 64 b itanium   microprocessor," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2002, pp. 276–504.

[2]. H. Partovi et al., "Flow-through latch and edge-triggered flip-flop hybrid elements," IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 138–139, Feb. 1996.

[3]. E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional push-pull pulsed latch with 726 Jops energy delay product in 65 nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2012, pp. 482–483.

[4]. V. Stojanovic and V. Oklobdzija, "Comparative analysis of master slave latches and flip-flops for high-performance and low-power systems," IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[5]. J. Montanaro et al., "A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor," IEEE J. Solid-State Circuits, vol. 31, no. 11, pp. 1703–1714, Nov. 1996.

[6]. S. Nomura et al., "A 9.7 mW AAC-decoding, 620 mW H.264 720p 60fps decoding, 8-core media processor with embedded forward body- biasing and power-gating circuit in 65 nm CMOS technology," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2008, pp. 262–264.

[7]. Y. Ueda et al., "6.33 mW MPEG audio decoding on a multimedia processor," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers Feb. 2006, pp. 1636–1637.

[8]. B.-S. Kong, S.-S. Kim, and Y.-H. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, pp. 1263–1271, Aug. 2001

[9]. C. K. Teh, T. Fujita, H. Hara, and M. Hamada, "A 77% energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40 nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2011, pp. 338–339.eeee