

Two-Stage Power Factor Correction Architecture For High Frequency Grid Operation

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Abstract - This project presents novel ac-dc power factor correction (PFC), power conversion architecture for single-phase grid interface. High efficiency, good power factor, and converter miniaturization, especially in low-to-medium power applications are the significance of this architecture. For converting power from the single-phase ac grid for dc loads must meet numerous, increasingly stringent requirements by Switched-mode rectifiers. Efficiency goals for ac-dc converters continue to rise. The architecture enables twice-line-frequency energy to be buffered at high voltage with a large voltage swing, enabling reduction in the energy buffer capacitor size, and elimination of electrolytic capacitors. New recommendations and future standards have increased the interest in power factor correction circuit. The proposed architecture is applied to an LED driver circuit converter operating at a (variable) HF switching frequency (3–10MHz) from 120Vac, and supplying a 35Vdc output at up to 30W. In addition, there has been a long desire for converter miniaturization (e.g., through the use of greatly increased switching frequencies to reduce the volume of energy storage elements). The prototype converter achieves high efficiency (95%) and power factor (0.9), and maintains good performance over a wide load range.

Key Words: ac-dc converters, high frequency, power factor correction (PFC), LED, soft charging switched capacitor....

1. INTRODUCTION

This paper presents a merged two-stage circuit topology suitable for either wide-range dc input voltage or ac line voltage at low-to-moderate power levels (e.g. up to 30W). High efficiency has always been a goal of power electronics. Moreover, high power factor (PF) is desirable to best convey real power from the ac grid to a dc load. While power factor has been traditionally considered important mainly at higher power levels, it is of increasing concern at lower power levels as well (e.g., 10's of watt), as reflected in goals for applications such as light-emitting diode (LED) drivers and laptop chargers. [6],[7]. This two-stage topology is based on a soft-charged switched-capacitor preregulator or transformation stage and a high-frequency magnetic regulator stage. Soft charging of the switched capacitor circuit, zero voltage switching of the high-frequency regulator circuit, and time-based indirect current control are used to maintain high efficiency, high power density, and high power factor. The proposed architecture is applied to

an LED driver circuit converter operating at a (variable) HF switching frequency (3–10MHz) from 120Vac, and supplying a 35Vdc output at up to 30W. The architecture enables twice-line-frequency energy to be buffered at high voltage with a large voltage swing, enabling reduction in the energy buffer capacitor size, and deletion of electrolytic capacitors. While this architecture can be beneficial with a variety of converter topologies. Moreover, we introduce circuit implementations that provide efficient operation in this range.

The prototype converter achieves high efficiency (95%) and power factor (0.9), and maintains good performance over a wide load range. Owing to architecture and HF operation, the prototype achieves a high 'box' power density of 50W/in³, with miniaturized inductors, ceramic energy buffer capacitors, and a small-volume EMI filter.

The dc-dc converter shows 88%–96% efficiency at 30-W power across 25–200V input voltage range, and the ac-dc converter achieves 88% efficiency with 0.9 power factor.

2. POWER FACTOR CORRECTION CIRCUIT

The proposed grid interface power conversion architecture comprises a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a power combining converter. The line-frequency rectifier draws current from the grid during a portion of the cycle, with a waveform controlled by the operation of the regulating converters. The capacitor stack provides most or all of the twice-line-frequency energy buffering, such that the converter can provide high power factor without buffering energy at the system output. One or more of the capacitors in the capacitor stack is relatively small, such that the total capacitor stack voltage can vary over a wide range as the line voltage varies over the line cycle. The input ac current waveform may approximate a clipped sine waveform or a similar waveform providing high power factor, while the total capacitor stack voltage closely follows the amplitude of the line voltage over the portion of the line cycle for which the rectifier conducts. A set of regulating converters, which have their inputs connected to capacitors of the stack of capacitors, provide regulated outputs. The currents drawn by the (at least) two regulating converters are modulated to draw energy from the capacitors, such that the currents drawn from the capacitor stack results in an input current waveform to the rectifier that provide both high power factor and the total needed energy transfer to support the output. Because the regulating converters operate from voltages that are much smaller than the total line voltage, they can be designed with switches having smaller voltage ratings than otherwise

possible (and having lower parasitic capacitance) at much higher frequencies and can be operated at smaller characteristic impedance levels than could a single converter rated at line voltage. For example, as the regulating converters may be very effectively implemented using resonant transition discontinuous mode inverted buck converters.

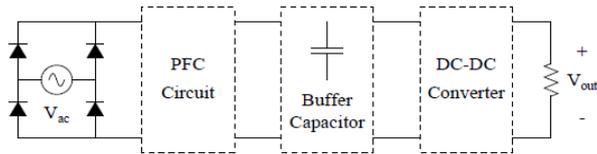


Fig -1: A conventional ac-dc power converter architecture.

This topology enables high-frequency (HF, 3–30 MHz) operation of the regulating converters with high efficiency, low device voltage stress, small component size, and good control capability. The power-combining converter has a multiplicity of inputs connected to the regulating converter outputs, wherein the power-combining converter draws energy from the regulating converter outputs and delivers the combined power to the converter system output. The power-combining converter may provide one or more of: voltage balancing among the regulating converter outputs, galvanic isolation, voltage transformation, a portion of twice-line-frequency energy buffering, and additional regulation of the output. The power-combining converter may be designed as a multi-input converter, or as a set of single-input converters which take inputs connected to ones of the regulating converter outputs and supply a single output. Because the power combining converter operates from a low, narrow-range input voltage, and may not need (in many designs) to provide regulation, it can be designed to be very compact. One possibility in this case is to design it for operation at HF or VHF. Another possibility is to design the power combining converter using switched-capacitor (SC) techniques. When the system does not require galvanic isolation, the SC circuit can be designed without magnetic elements, and has benefits including high efficiency and small size. An ac source can produce an ac voltage with low frequency such as the standard 50/60-Hz utility voltage frequency, or an ac voltage with high frequency such as 100 kHz. In both cases, the most efficient utilization of power will occur when the current flowing out of the source is sinusoidal and in phase with the source voltage. Given the nature of the two types of sources, however, techniques that are appropriate for one type of source are not appropriate for the other.

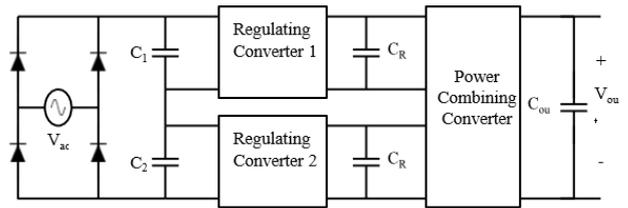


Fig-2: The proposed grid interface power conversion architecture comprises a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a power combining converter.

The proposed grid interface power conversion architecture comprises-

- A. Line-frequency rectifier
 - B. A stack of capacitors
 - C. A set of regulating converters
 - D. Power combining Converter
- A. **Line-frequency rectifier**-The line-frequency rectifier draws current from the grid during a portion of the cycle, with a waveform controlled by the operation of the regulating converters.
 - B. **Stack of capacitors**-One or more of the capacitors in the capacitor stack is relatively small, such that the total capacitor stack voltage can vary over a wide range as the line voltage varies over the line cycle. One of the capacitors (e.g., C2) buffers most of the twice-line-frequency energy, while the other capacitor (e.g., C1) is much smaller, and simply acts as a bypass capacitor for its associated high-frequency switching stage. One capacitor is thus sized principally based on line-frequency energy buffering, while the other is sized principally based on switching frequency considerations.
 - C. **Set of regulating converters**-This topology enables high-frequency (HF, 3–30MHz) operation of the regulating converters with high efficiency, low device voltage stress, small component size, and good control capability.
 - i. **Boost converter**- A boost converter is often selected for the PFC circuit because of its filtered input current, high efficiency, and high power factor capability[3]-[5]. This approach may yield high efficiency and very high power factor, but it is not amenable to converter miniaturization in low dc voltage and low-to- medium power applications, because It is hard to greatly reduce the volume of the boost circuit (e.g., through high- frequency operation) owing to loss limits, large inductance (i.e., high characteristic impedance level), and large

parasitic capacitance levels (e.g., large output capacitance of the switch)[1], and the following dc-dc converter operates at high voltage and has a large step-down voltage conversion ratio, so that it is again difficult to be designed at high frequency with small volume, and the volume of the energy buffer capacitor is large.

- ii. **Buck converter-** One alternative circuit topology for the PFC circuit is a buck converter, which can draw a clipped-sinusoidal current waveform with 0.7–0.9 power factor, suitable for many applications[13]-[15]. A benefit of the buck PFC circuit for low-output-voltage applications is reduced voltage stress and voltage conversion ratio for the following dc-dc converter.

D. **Power combining Converter-**The power-combining converter may provide one or more of: voltage balancing among the regulating converter outputs, galvanic isolation, voltage transformation, a portion of twice-line-frequency energy buffering, and additional regulation of the output. The power-combining converter may be designed as a multi-input converter, or as a set of single-input converters which take inputs connected to ones of the regulating converter outputs and supply a single output. Because the power combining converter operates from a low, narrow-range input voltage, and may not need (in many designs) to provide regulation, it can be designed to be very compact. One possibility in this case is to design it for operation at HF or VHF. Another possibility is to design the power combining converter using switched-capacitor (SC) techniques.

Advantages

1. The prototype converter achieves high efficiency (95%) and power factor (0.9), and maintains good performance over a wide load range.
2. The proposed grid interface architecture has several advantages. One apparent significance is the decreased voltage stress to the components in the regulating converters and the power combining converter relative to the line voltage. In comparison to conventional grid interface converters which must be rated for the grid voltage, each regulating converter of the proposed architecture instead operates only up to about half of the grid voltage because of the stacked capacitor structure.
3. The power combining converter, tied to the regulated outputs of the regulating converters,

operates at both low voltage and narrow input voltage range.

4. Proposed approach gives high-frequency operation and miniaturization of converter with high efficiency .
5. Significant efficiency and miniaturization advantage for low voltage applications.
6. It enables substantial increases in operating frequency as compared to conventional designs, enabling a further degree of miniaturization. Less financial burden correcting mistakes.
7. Higher switching frequencies (bounded by practically achievable capacitance levels) are enabled.
8. High frequency operation further helps converter miniaturization with the reduced EMI filter requirements.
9. Demonstrating the value of emerged two-stage architecture to provide substantial design benefits in high-input voltage, low-power step down conversion applications ,including both wide-range-input dc-dc and line-input ac-dc systems.

3. CONCLUSION

The proposed stacked combined architecture significantly decreases the voltage stress of the active and passive devices and reduces characteristic impedance levels, enabling substantial increases in switching frequency when utilized with appropriate converter topologies. Moreover, good power factor is achieved while dynamically buffering twice-line-frequency ac energy with relatively small capacitors operating with large voltage swing. The prototype converter achieves high efficiency and good power factor over a wide power range.

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