

Robust Reversible Multiplexer Design using Mach-Zehnder Interferometer

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Abstract - Low-power design techniques has an increased emphasis with the advancements in semiconductor technology over the last few decades. Reversible computing has been proposed by several researchers as a possible alternative to address the energy dissipation problem. Adiabatic logic, nuclear magnetic resonance, optical computing are the implementation alternatives for reversible logic circuits that have been explored in recent years. Recently researchers have proposed implementations of various reversible logic circuits in the all-optical computing domain. Most of these works are based on semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI), which provides desirable features like low power, fast switching and ease of fabrication. In this paper we present an all-optical implementation of a digital multiplexer using MZI switches. Both non-reversible and reversible versions of multiplexer design are proposed, along with analytical evaluation of the design complexities both in terms of delay and resource requirements. The final optical netlists obtained have been compared against traditional reversible synthesis approaches, by using an available synthesis tool and then mapping the reversible gates to MZI switch based implementations.

1. INTRODUCTION

Reversible logic is becoming a popular emerging paradigm because of its applications in various emerging technologies like quantum computing, DNA computing, optical computing, etc. It is also considered as an alternate low-power design methodology. A reversible circuit consists of a cascade of reversible gates without any fanout or feedback connections, and the number of inputs and outputs must be equal. There exists various ways by which reversible circuits can be implemented like NMR technology, optical technology, etc. In the optical domain, a photon can store information in a signal having zero rest mass and provide very high speed. These properties of photon have motivated researchers to study and implement reversible circuits in optical domain. Theoretically from the decade old principles of Landauer and Bennett, reversible logic is considered as a potential of reversible gates can be one possible alternative to

overcome the power dissipation problem in conventional computing. In recent times researchers have investigated various reversible logic gates and their all-optical implementations using microresonator and semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI) switch. Also MZI-based implementation of reversible logic gates offer significant advantages like ease of fabrication, high speed, low power, and fast switching time. In this paper, an all-optical implementation methodology of reversible multiplexers has been proposed. Delay analysis in implementing arbitrary functions using such multiplexers have also been discussed.

2. LITERATURE SURVEY

In this section we briefly discuss some relevant background about MZI-based optical switch, various reversible gates, and their all-optical implementations.

A. MZI-based all-optical switch

Mach-Zehnder interferometer (MZI) is one of the efficient configurable building blocks in optical computing. Some of the main advantages for using MZI switches in various circuit design methodologies are their compact size, ease of fabrication, thermal stability and fast switching time. Recently optical switches based on MZI have attracted many researchers in the area of all-optical reversible logic implementations. An all-optical MZI switch can be constructed using two SOA and two couplers. SOA amplifies an optical signal without converting it to electric signal and uses a semiconductor to administer the gain medium. A coupler is a passive optical component which can either combine or split a signal based on application requirement. It consists of two input ports and two output ports. At the input port, the optical signal entering at port A is called the *incoming signal* (λ_1) and the optical signal coming from port B is termed as *control signal* (λ_2). The output ports are termed as *bar port* and *cross port*. The switch works as follows.

- When both incoming signal (λ_1) at A and control signal (λ_2) at B are present, there will be a presence of light at *bar port* and no light at *cross port*.

- When there is incoming signal (λ_1) at A and no control signal (λ_2) at B, then there is absence of light at *bar port* and presence of light at *cross port*.

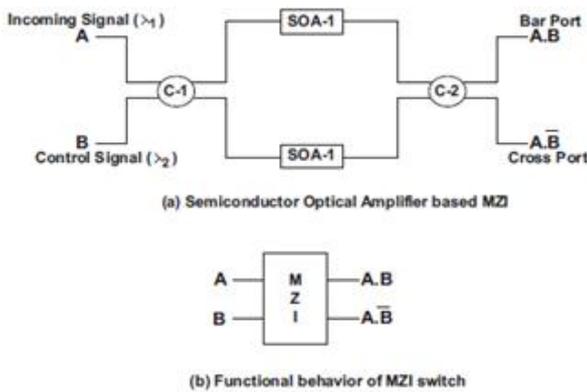


Figure: SOA based MZI switch

C. Implementing reversible gates using MZI switch

Several researchers have studied and proposed all-optical implementations of reversible and non-reversible gates like Toffoli, Fredkin, Peres, XOR, NOR, etc, and some function implementations like adder [9] and signed adder [1]. In all the works, the *optical cost* of implementation has been estimated as the number of MZI switches required, since the costs of beam splitters and beam combiners are relatively small. And the delay has been calculated as the number of stages of MZI switches multiplied by a unit Δ .

3. PROPOSED ALL-OPTICAL MULTIPLEXER DESIGN

In this section, we present the all-optical implementation of a digital multiplexer using MZI switches, beam splitters and beam couplers. In the following subsections, we discuss the design of a (2×1) non-reversible all-optical multiplexer, followed by its generalization to $(2n \times 1)$ multiplexer. Then a design extension to make the multiplexer design reversible is suggested, that requires one additional ancilla line.

A. Design of (2×1) multiplexer

The schematic diagram of a (2×1) multiplexer is shown in Figure 4(a), where I_0 and I_1 are the two inputs, and S is the select line. The function implemented at the output is also shown.

The all-optical implementation of the multiplexer is shown in Figure 4(b), which consists of a beam splitter (BS) for splitting the select input S , two MZI switches which generates the sub functions $I_0.S$, $I_0.S'$, $S.I_1$ and $S.I_1'$ respectively, and finally a beam coupler (BC) that combines two of the MZI outputs to realize the desired functionality at the final output F . The BC essentially performs the logical OR function in the digital domain.

In the earlier reported works on implementing logic functions using MZI switches, BS and BC [8], [9], the cost of implementation (referred to as *optical cost*) has been estimated as the number of MZI switches required, as the relative costs of BS and BC are small. Similarly, the delay is measured as the length of the longest cascade of MZI switches. Denoting the units of cost and delay by MZI and Δ , for the implementation as shown in Figure 4(b),

$$M(1) = 2 \text{ MZI}$$

$$D(1) = 1 \Delta$$

where $M(x)$ and $D(x)$ respectively denote the optical cost and delay for a $(2x \times 1)$ multiplexer.

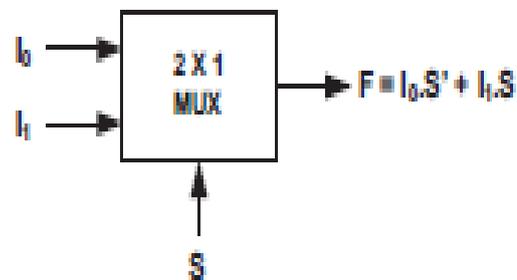


Figure: A 2- to-1 MUX

B. Design of $(2n \times 1)$ multiplexer

We now show how a multiplexer of any larger size can be constructed using smaller multiplexers as basic building blocks. This is a standard approach followed in conventional logic design; however, in the context of the present work, we shall be analyzing the costs and delays with respect to the all-optical implementations.

A (4×1) multiplexer can be constructed using three (2×1) multiplexers, as shown in Figure, where I_0, I_1, I_2, I_3 are the inputs, S_0, S_1 are the select lines, and F is the output. Each of the three multiplexers can be replaced by their corresponding all-optical netlists, to get the

final netlist as shown in Figure For this implementation,

$$M(2) = 6 \text{ MZI}$$

$$D(2) = 2 \Delta$$

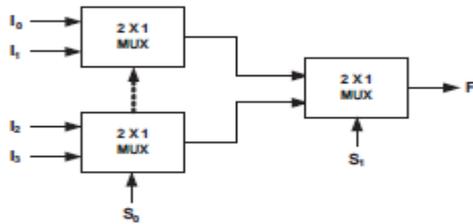


Figure: Schematic diagram of 4-to-1 MUX

Similarly, an (8×1) multiplexer can be built using two (4×1) and one (2×1) multiplexers, for which

$$M(3) = 6 * 2 + 2 = 14 \text{ MZI}$$

$$D(3) = 3 \Delta$$

Generalizing, an $(2n \times 1)$ multiplexer can be built using two $(2n-1 \times 1)$ and one (2×1) multiplexers. We have seen earlier that $M(1) = 2$, $M(2) = 6$, and $M(3) = 14$. We can express the optical cost $M(n)$ as a recurrence relation and solve it as follows

$$\begin{aligned} M(n) &= 2.M(n-1) + M(1) \\ &= 2.M(n-1) + 2 \\ &= 2[2.M(n-2) + 2] + 2 = 22.M(n-2) + 22 + 2 \\ &= 22[2.M(n-3) + 2] + 22 + 2 \\ &= 23.M(n-3) + 23 + 22 + 2 \\ &\dots \\ &= 2n-1.M(1) + 2n-1 + 2n-2 + \dots + 2 \\ &= 2n + 2n-1 + \dots + 2 \\ &= (2n+1 - 2) \text{ MZI (1)} \end{aligned}$$

Since the number of MZI stages is equal to the number of multiplexer select lines in the final netlist, we can write the delay for an $(2n \times 1)$ multiplexer as

$$D(n) = n \Delta \text{ (2)}$$

C. Reversible implementation of the multiplexer

The all-optical implementations of multiplexer as discussed in the previous subsection are not reversible. One possible approach to have a reversible implementation of a multiplexer is to define a suitable reversible embedding for a (2×1) multiplexer, and use it to build larger multiplexers.

A. Optimization rules

It may be observed that in the all-optical multiplexer-based realization of functions, some of the MZI switches have constant inputs (0 or 1). Some of these MZI switches may be eliminated from the final netlist. These may be summarized in terms of the following four optimization rules.

- a) If the upper input of a MZI switch is 0, both the outputs will be 0's and the switch can be deleted from the netlist.
- b) If the lower input of a MZI switch is 0, the upper output will also be 0, and the upper input will get copied to the lower output. In this case also, the MZI switch can be deleted
- c) If the upper input of a MZI switch is 1, the two outputs will be respectively the lower input and its complement. A MZI switch in this configuration can be used as an Inverter
- d) If the lower input of a MZI switch is 1, the upper input gets copied to the upper output, and the lower output becomes 0. Here again the switch can be deleted.

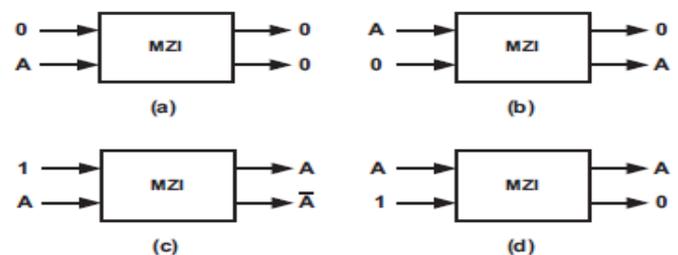


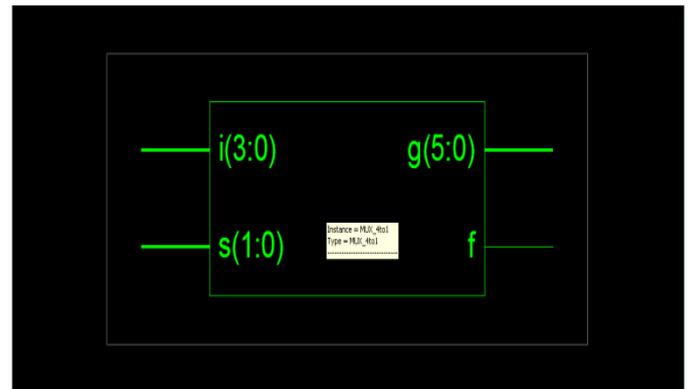
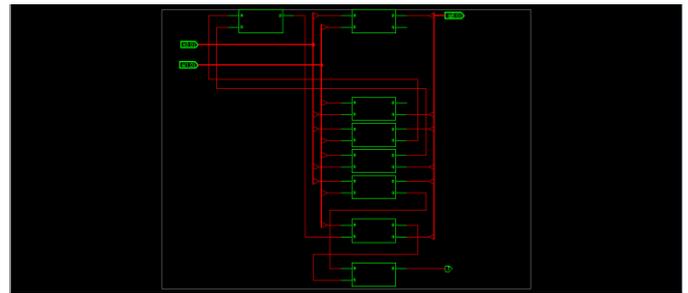
Figure: The optimization rules

4. EXPERIMENTAL RESULTS

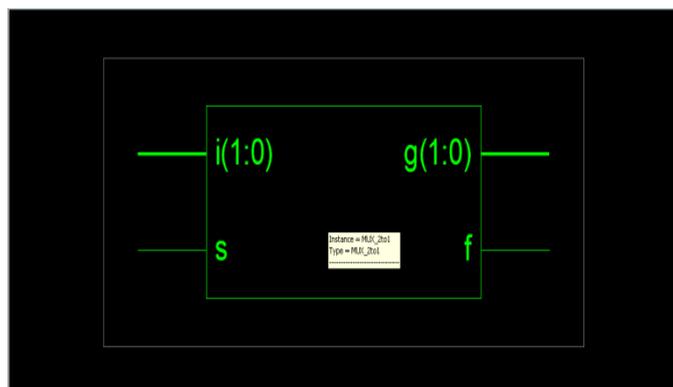
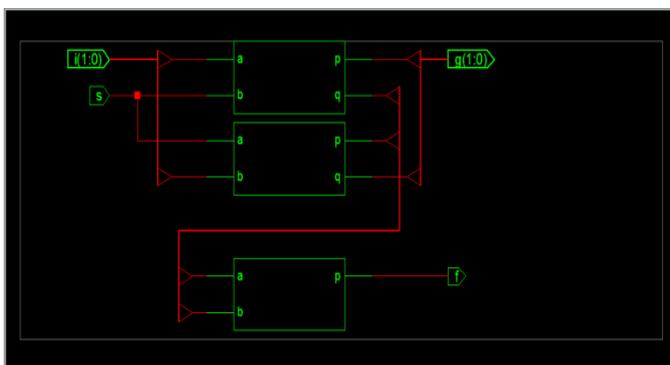
A summary of the results has been tabulated in Table. The tabular form represents the parameters of the normal & MZI based multiplexers. The figures below

represent the schematic diagrams of MZI based 2-to-1 & 4-to-1 multiplexers.

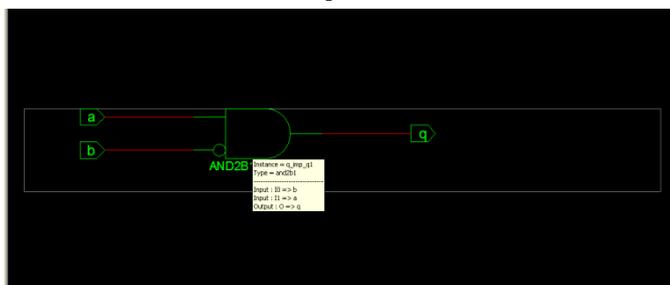
It may be noted that the delay as reported in table for the proposed approach uses a straightforward multiplexer based realization without using the optimization rules as discussed in the previous section. If the rules are used, significant reductions in the number of MZI switches are expected. The table shows that the optical costs for some of the benchmarks are less in the proposed approach, while for some others it is more. However, the delays are significantly less for all the benchmarks in the multiplexer based approach.



Figures: Schematic diagrams of MZI based 4-to-1 multiplexer



Figures: Schematic diagrams of MZI based 2-to-1 multiplexer



Parameters	Normal multiplexer	MZI based multiplexer
Delay for 4x1 multiplexer	7.303ns	7.249ns
Delay for 2x1 multiplexer	7.2ns	7.111ns
No. of 4 input LUT'S used for 4X1 multiplexer	2	7
No. of occupied slices for 4x1 multiplexer	1	4
Total no. of 4 input LUT'S for 4x1 multiplexer	2	7
No. of bonded IOB'S for 4x1 multiplexer	7	13
No. of 4 input LUT'S used for 2x1 multiplexer	1	3
No. of occupied slices for 2x1 multiplexer	1	2
Total no. of 4 input LUT'S for 2x1 multiplexer	1	3
No. of bonded IOB'S for 2x1 multiplexer	4	6

Table 1
Parameters of normal and MZI based multiplexers

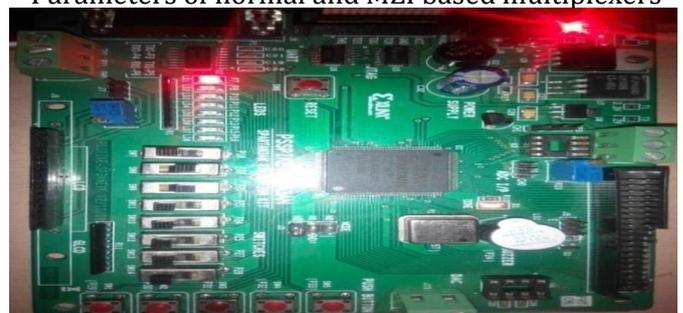


Figure: Verification on Spartan3AN evaluation kit

5. CONCLUSION

In this paper all-optical implementation of multiplexers using Mach-Zehnder Interferometer (MZI) based switches have been presented, along with analysis of the corresponding costs and delays. Using one ancilla line, a reversible implementation of multiplexer is also proposed. A method for reversible implementation of functions using MZI switches and some optimization rules have also been presented. Experimental results for some of the benchmarks reveal that the proposed all-optical implementation results in significantly less delay as compared to the one based on conventional reversible gate implementations. Comparison with a recent work for the 13 standard 3-variable functions has also been reported, which demonstrates significant improvements both in terms of optical cost and delay.

6. REFERENCES

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