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A Low Noise Two Stage Operational Amplifier on 45nm CMOS Process

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Abstract – ***A new low voltage and low power two stage operational amplifier which describes different parameters as Gain, Phase margin, Noise, SFDR and THD under 45nm CMOS technology. Implementations have been done in Tanner EDA software V14.1. Circuit designed in S-edit and simulations done with the help of T spice. Waveforms have been obtained in W-edit. In this paper operational amplifier designed on 45nm technology CMOS process with 1.2V power supply and achieved very good phase margin and 6.10db gain with low noise has been achieved.***

Key Words: *Op-amp, Gain, CMOS, Phase margin and Miller capacitance.*

1. INTRODUCTION

To see rapid and fast growth in technology electronic engineers has motivated to implement various devices which have high speed and consumes low power supply. Because of simple characteristics and robustness, two stage op-amp generally used. Also its design implementation is very easy with the help of Tanner software V14.1. For closed loop stability frequency compensation technique is necessary to use because negative feedback connection used in op-amp. By reducing supply voltage or total current power dissipation can be reduced. By choosing proper aspect ratio W/L and proper biasing optimize op-amp can be designed.
There are various biasing techniques. Earlier voltage biasing used but now a days current biasing dominates.
When MOS devices operate in saturation region high gain can be achieved.

As in new generation of CMOS technology, it tends to keep short transistor channel length and scaled down supply voltage as well becomes a challenge for the designers. Operational amplifier has direct coupling and has high gain, low noise device. It is a versatile device that can be used to amplify ac as well as dc input signals [1].

1.1 Miller capacitance

In this method a coupling capacitor Cc is connected in parallel with the second stage op-amp. According to Miller's theorem, the impedance supplied by two voltage sources connected in series, may be split into two grounded elements with corresponding impedances [2]. Since in this case, the impedance is purely capacitive and second stage of op-amp has inverting gain, the first capacitor Cc has large capacitance needed to reduce the pole of the first stage on left side of the imaginary axis. It can be generated by a smaller capacitor and described by Miller multiplication [3] [4]. The second capacitor has a value which is very much close to the compensation capacitor (Cc) which is connected at the output of the amplifiers stage. Now pole splitting occurs, thus dominant pole compensation has been achieved [5] [6].
To achieve high gain two cascaded stages of operational amplifier are required. For achieving high gain, high precision also required for many applications. The first challenge is to provide small supply voltage for op-amp which limits the enough output voltage in the cascaded op-amp and so as signal to noise ratio decreases. So obtaining high gain at low power supply is tough job for researchers [7].

1.2 Aspect Ratio (W/L)

Aspect ratio is the ratio of width to length of the MOS devices. The following two thumb rules are kept in mind while choosing the aspect ratio (W/L) of MOS devices. First, L of PMOS should be roughly double of NMOS to get the maximum possible gain.
Second, for achieving high gain and high gain margin W/L should also be high. After taking the above written facts into account and many times careful iteration increases the probabilities of achieving high gain.
It is also important to note that when W/L increases output voltage increases too. But it is very tough to choose width and length of MOS devices to achieve same voltage what voltage is given to input.
Table 1 shows the different combination of aspect ratios used for present work.

Table -1: W/L for PMOS and NMOS devices

PMOS DEVICES	W/L	NMOS DEVICES	W/L
PMOS_1	100	NMOS_1	12.5
PMOS_2	1000	NMOS_2	12.5
PMOS_3	1000	NMOS_3	12.5
PMOS_4	333.33	NMOS_4	12.5
PMOS_5	333.33	NMOS_5	12.5

2. BLOCK DIAGRAM OF TWO STAGE OP-AMP

For achieving high gain two stage cascaded op-amp circuit employed. The general block diagram of an op-amp, with a differential amplifier, compensation circuit and biasing circuit, is shown in Fig 1. Output is taken from common source amplifier. Differential amplifier means amplifier which amplifies two different voltages which are applied on vin+ and vin- terminals. Compensation circuitry is very useful for compensate the swing of output voltage. For this coupling capacitors Cc are used. Biasing circuit usually used to fix Q point in proper region. So that device will operate in required region and give best outputs.

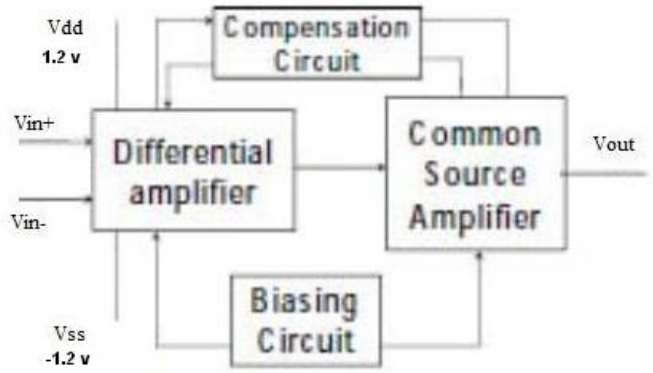

Fig -1: Block diagram of two stage CMOS op-amp

The block diagram is shown in Fig 2. The first block is a differential amplifier having two inputs as vin+ and vin-. One is the inverting and other is the non-inverting terminal. Two different voltages can apply on both the terminals. The differential amplifier amplifies a differential voltage or a differential current at the output, which depends only on differential input voltage or currents. The next block is a second gain stage. It is used to convert the differential voltage into amplified form at single terminal with capacitor.

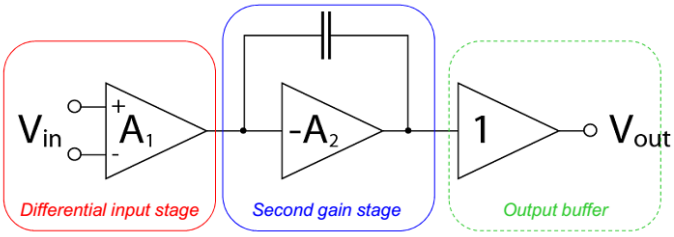

Fig -2: Simplified block diagram

The gain provided by the input (first) stage does not suffice, so an additional amplification is required which is called as the second stage. Here second stage (common source amplifier) provides the required extra gain. The op-amp is connected with small capacitive load in compensation circuit. The main aim of the compensation circuit is to maintain stability. It will occur when the gain would be at high frequencies and also by negative feedback applied on the op-amp.

A few steps were taken into account to increase the open-loop gain. First is to decrease the width mirroring MOSFET, PMOS1, so that it would cause a large mirror of currents to the both stages. Second, the differential positive and negative transistors had their widths increased. By increasing widths op-amp will give large gain margin for the first stage as the first stage of the op-amp had a lower gain margin.

3. SCEMATIC DIAGRAM AND ANALYSIS OF OP-AMP

In designing an op-amp, various characteristics, as unity gain bandwidth, gain margin, phase margin, SFDR and THD all have to be taken into considerations. To obtain closed loop stability and to obtain high gain, frequency compensation with negative feedback is required for op-amp designs. So that slew rate enhanced and power dissipation reduced by reducing supply voltage. The power dissipation is reduced so as dynamic range. So it becomes difficult to keep MOS devices in saturation mode with that available voltage. Another concern is the threshold level of supply voltage of the transistor. As decrease in supply voltage below threshold level causes biasing issues. In order to achieve the required degree of stability or say phase margin, other parameters would be compromised. To design of an op-amp, a good compensation strategy and design methodology required. In the present paper low voltage used so slew rate is small. By using the same technique slew rate is improved, as well as lower power dissipation is achieved. Slew rate is change in voltage with respect to change in unit time [8].

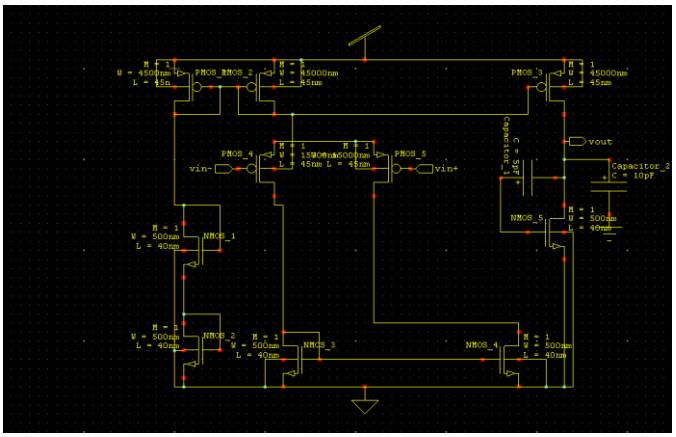

Fig -3: Schematic diagram of 2 stage CMOS op-amp

4. SIMULATION RESULTS

The simulations have been done on design using 45nm CMOS technology on Tanner EDA V14.1 software and results obtained in terms of wave forms. Schematic had been drawn on S-edit. Codes had written on T-spice and in W-edit results can be seen.

4.1 Transient Analysis

vdd=1.2v and vss=-1.2v
C1=5pf and C2=10pf
After simulation output voltage will be 0.92v. Spurious free dynamic range (SFDR) became 8db at 20MHz and Total Harmonic Distortion (THD) became -43.16dB and slew rate would be 62.8v/µs.

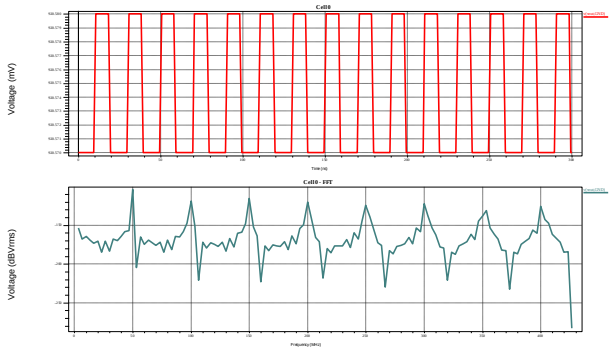

Fig -4: Transient response (i) vout=0.92v (ii) FFT performance SFDR=8db at 20MHz

Obtaining various parameter as SFDR, THD, slew rate gain and phase by 45nm as follows.

Table -2: Present work with 45nm

Parameters	45nm
vdd(v)	1.2
Gain(dB)	6.1
vout(v)	0.92
SFDR(dB)	8
THD	-43.16
Slew rate (v/µs)	62.8

By table it has been observed that output of transient response achieved what input voltage given to circuitry.

4.2 AC Analysis

In AC analysis for obtaining results put vdd=2.3v, vss=-2.3v and ac=2v. Apply vin+=9mv and vin-=1mv. Result of Gain is 6.10db and phase margin is 1.152 e+002. Gain cross over or unity gain bandwidth is 3.3GHz as noticed in Fig -5.

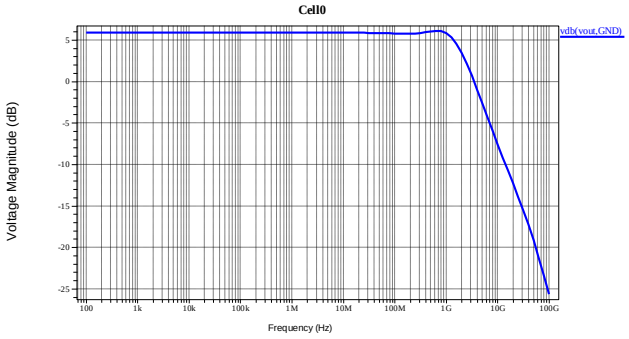

Fig -5: Frequency response curve of op-amp for Gain=6.10db

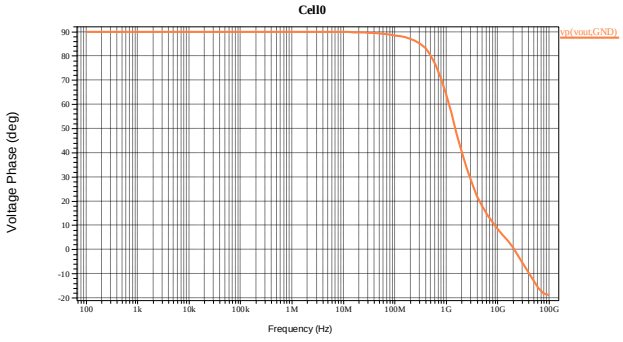

Fig -6: Frequency response curve for Phase

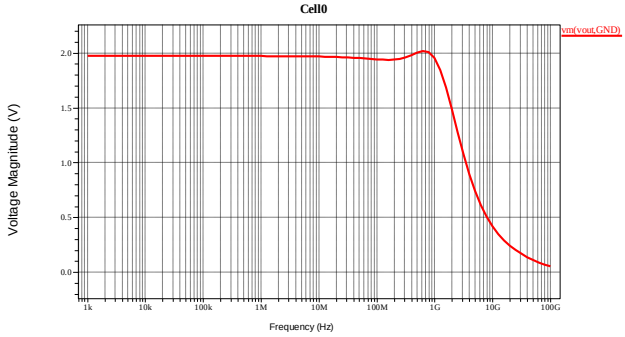

Fig -7: Output voltage (magnitude)

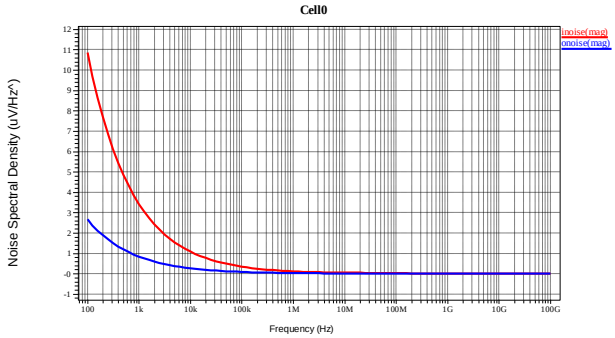

Fig -8: Input and Output Noise comparison

4.3 DC Analysis

vdd=1.2v

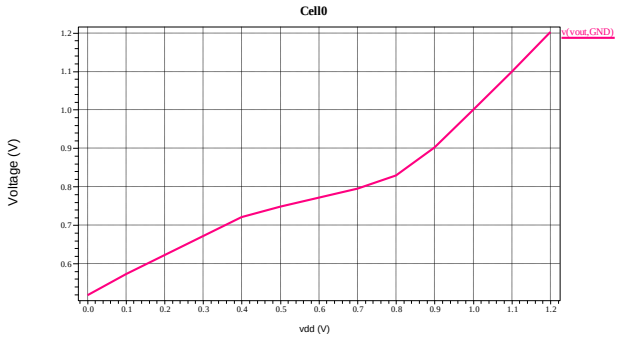

Fig -9: DC response

5. CONCLUSIONS

In this paper, two stage operational amplifier with 1.2v supply in 45nm CMOS technology presented. By miller capacitance gain can be enhance and good phase margin achieved.

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BIOGRAPHIES

Shruti Pancholi (B.E, M.Tech, and pursuing Ph.D) has 11 years experience of teaching. She has published 2 papers in international Journal and 1 international conference.

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