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AREA EFFICIENT LOW ERROR COMPENSATION MULTIPLIER DESIGN USING FIXED WIDTH RPR

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ABSTRACT

In area efficient low error compensation multiplier design is using fixed width RPR(Reduced Precision Redundancy). We propose a new method called fixed width RPR for DSP applications. This fixed width multiplier is placed in ANT architecture to meet high speed, low power consumption and area efficiency. The fixed RPR is designed with compensation circuit for minimizing the occurrence of error. The nxn bit is used as a input. The partial product term is used in RPR block for input correction vector and trivial input modification vector to worse the truncation errors. To achieve more precise error compensation. Variable correction value is used the truncation error can be compensation circuit is minimized.

KEY WORDS

Algorithmic noise tolerant (ANT), fixed-width multi-plier,reduced-precision replica (RPR),voltage overcalling(VOS) and error correction block(EC)

1. INTRODUCTION

To lower the power indulgence, supply voltage scaling is broadly used as an effective low power technique. The power utilization in CMOS circuits is comparative to the square of supply voltage. The ANT architecture contains both main digital processor and error correction block. In ANT design we propose a fixed width RPR instead of full width RPR. RPR stands for reduced precision replica, if the original system computes the error,

the RPR output is taken as the corrected output. To achieve more precise compensation, we construct the error compensation circuit mainly using the partial product term with largest weight in the LSB segment. By using compensation circuit we truncate the error with the help of variable correction vector. The disadvantage of the previous method is hardware complexity is high, voltage over scaling is used to reduce the error. This can be overcome by RPR method.

2. ANT DESIGN

ANT can be mainly divided into Prediction based ANT and Reduced Precision Redundancy based ANT. Using ANT technique to recover the concert of DSP algorithms in presence of bit error rates. Therefore ANT can produce more efficient signals. ANT to balance for deprivation in the structure production due to errors from soft computations.

3. FULL WIDTH MULTIPLIER DESIGN

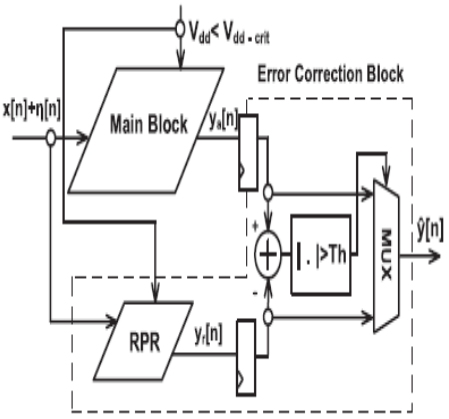


Fig. 1 ANT architecture using

This technique consists of main block and error correction block. To meet ultralow power demand. In

the ANT method a duplication of the MDSP(Main Digital Signal Processor) but with condensed precision operands and shorter computation delay is used as EC block. The input is given to the main block it process to produce the output as ya[n]. RPR block simultaneously processed and produce the output as yr[n]. RPR output yr [n] is still correct since the critical path delay of the replica is smaller than Tsamp. Therefore, yr [n] is applied to detect errors in the MDSP output ya[n]. The error in the output is corrected by using voltage overscaling Error detection is accomplished by comparing the difference |ya[n] − yr [n]| against a threshold Th. Once the difference between ya[n] and yr [n] is larger than Th, the output ˆy[n] is yr [n] instead of ya[n]. As a result, ˆy[n] can be expressed as

ˆy[n] = ya [n] ,
if |ya [n] − yr [n]| ≤ Th yr [n],
if |ya [n] − yr [n]| > Th……..(1)
Th is determined by
Th = max |yo [n] − yr [n] |…….. (2)
Where yo[n] is error free output signal

4. PROPOSED FIXED WIDTH MULTIPLIER

The fixed-width multipliers have been widely used in digital signal processor(DSP) design due to their lower power dissipation and less area. In order to reduce the chip area many fixed width Booth multipliers have been used. They decrease the detection accurateness because of reduced partial products. This method can reduce the truncated error by using variable compensation value. In order to overcome the disadvantages we presented a method of dividing the reduced partial products into the foremost truncated section and the trivial shortened section.

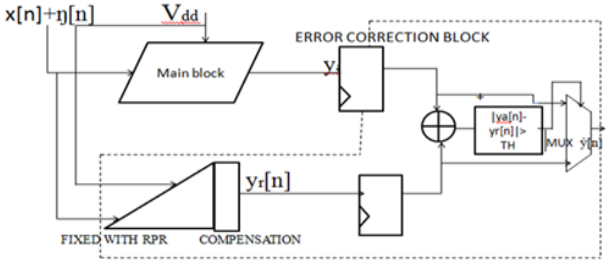


Fig. 2 proposed ANT architecture

The main block is implemented with the help of power supply VDD. The output of the main block is produced and it is denoted by ya[n]. Simultaneously the RPR block also implemented the compensation circuit correct the truncated error and produce the output. The output of this block is denoted by yr[n]. Both the outputs are taken into the decision block. The threshold value is predefined we compare the both outputs ya[n] and yr[n]. The value is less than the threshold value the multiplexer produce the output as main block ya[n].It is consider as error free output. If the value is greater than the threshold value the multiplexer produce the output as yr[n].It is consider as error truncated value. The soft error in the output is minimized.

4.1. MAIN BLOCK

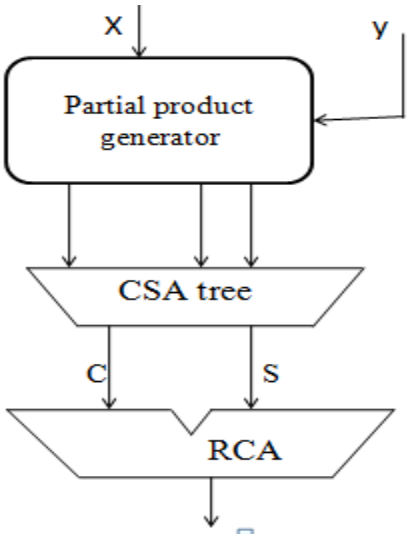


Fig. 3 Main Block diagram for proposed ANT design

In main block we are given nxn inputs to the partial product generator. The generator circuit generate the partial product terms. The output of the circuit is given to the CSA (Carry Save Adder)tree.CSA circuit group the product terms to produce two row outputs carry and sum bits. This process is iterated until all the partial product terms are grouped. Finally the output of CSA tree is given to the RCA(Ripple Carry Adder)circuit. The RCA circuit is processed based on the inputs size they finally produce the output of the main block. is operated with the help of power supply and its output is denoted by ya[n].

4.2. ERROR CORRECTION BLOCK

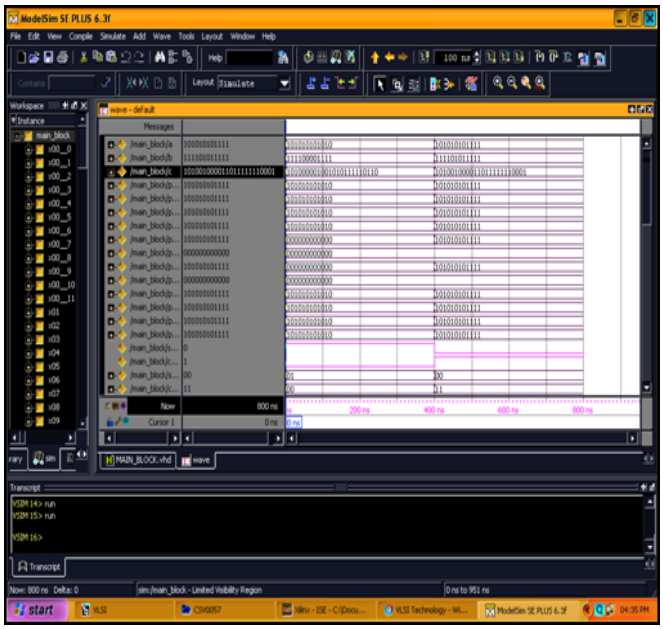
The error correction hunk which consist of multiplexer, RPR block compensation circuits and

registers. In error correction block the inputs are given to the RPR block. The function of the RPR block is to correct the errors occurring in the output. The RPR hunk take the input as partial products. If the input is 12x12 bits it takes half of the partial terms or MSB segments. The RPR only takes 6 bits for processing. Error in the output is minimized or truncated. After that the compensation circuit to compensate the truncated errors and finally produce the input we use RPR method. Mutually the outputs are taken to the decision block. This hunk is used for selecting the error free production. Mutual values are compared with threshold value the ultimate value is displayed. If the value is greater than the threshold value the RPR value is displayed or else main block output is displayed. This output is considered as a error free output. With the help of selection line the multiplier choose the correct output. The variable precision value is used to achieve good precision value. The input correction vector is used in error compensation circuit for compensating the errors. The error in the output is minimized.

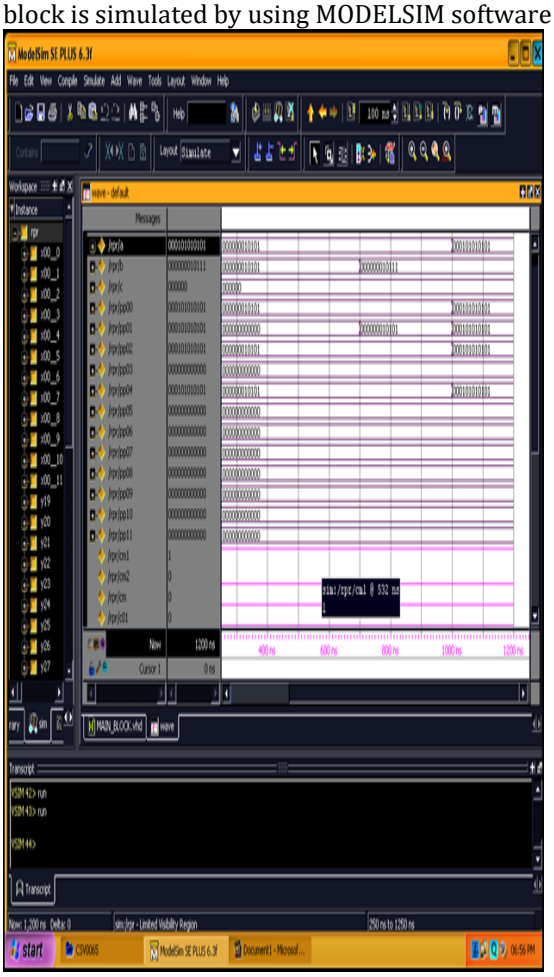
5. SIMULATION RESULTS AND DISCUSSION

In this zone, we converse about the concert of the proposed RPR ANT structure.

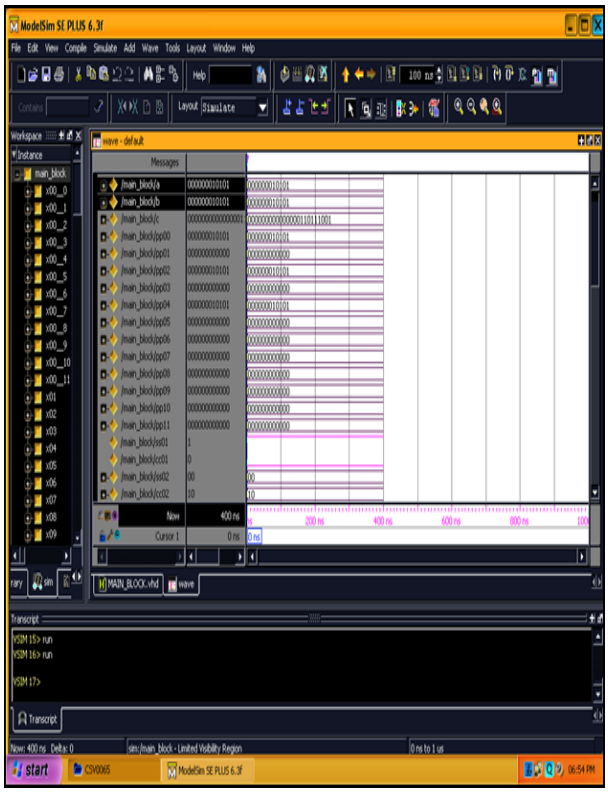
First, we define the main block, it is simulated by using MODELSIM software .Here two inputs are x and y.



Second, we define the EC block, error correction block is simulated by using MODELSIM software



Finally we define whole circuit output waveforms that is simulated by using MODELSIM software



6. CONCLUSION

In order to evaluate the performance of design ,we have to compare the performance of this fixed width RPR design with previous full width RPR design. The design is synthesized by using Xilinx 8.1V.based on this modification soft digital signal processing systems that consume much less power than systems operating error-free at critical supply voltages Soft digital signal processing systems can reduce leakage power and provide robustness to errors caused by leakage currents.

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