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BDD-based implementation of low power 32-bit CRC encoder and decoder

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Abstract - ***This paper presents the implementation of BDD- based 32-bit CRC encoder and decoder using LFSR methodology, with low power and less area. Generally 32-bit CRC is used in Ethernet frame for fault recognition at the transmitted data. The functional required for LFSR implementation is shift registers, flip flop which works for high frequency and yields less delay and consumes less power, the TSPC flip flop which is suitable for high speed and low power is modified and XOR gate is designed by using BDD (binary decision diagram) based approach which provide 58% improvement in power. Proposed design of 32-bit CRC is implemented in Cadence virtuoso tool using GPDK 180nm CMOS technology, with supply voltage of 1.8V.***

Key Words: *Cyclic Redundancy Check, Linear Feedback Shift Register, Binary Decision diagram (BDD), TSPC flip flop, low power, low area.*

1. INTRODUCTION

Computerized correspondence framework is utilized to transport a data bearing signal from the source to a client destination through a correspondence channel and each correspondence framework attempt to verify that broadcast data achieve the destination with no slip. For reliable transmission of data detection of error is necessary.

In networking systems a significant role of the data link layer is to convert the potentially unreliable physical link between two machines into an apparently very reliable link. This is achieved by including redundant information in each transmitted frame. Depending on the nature of the link and the data, one can include just enough redundancy to make it possible to detect errors and then arrange for the retransmission of damaged frames. The cyclic redundancy check (CRC) is a widely used parity based error detection scheme in serial data transmission.

Applications that necessitate additional assurance, for example, Department of Defense applications, utilize 32 or 64-bit CRC. Main application of CRC is in Ethernet frame for error detection at the transmitted data [1].

32-bit CRC polynomial for Ethernet applications is:

CRC32:0X04C11DB7=$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$

2. PROPOSED 32-BIT CRC ENCODER AND DECODER ARCHITECTURE

32-bit CRC encoder and decoder which is presented in Figure (1) is implemented using LFSR with the help of 32-bit CRC polynomial. A 32-bit LFSR is a 32-bit length shift register with feedback to its input. The feedback is formed by XORing or XNORing the outputs of selected stages of the shift register - referred to as 'taps' - and then inputting this to the least significant bit (stage 0)[2]. This 32-bit CRC architecture consumes less power and yields less delay by modifying TSPC flip flop circuit using split output concept and XOR gate circuit using BDD approach.

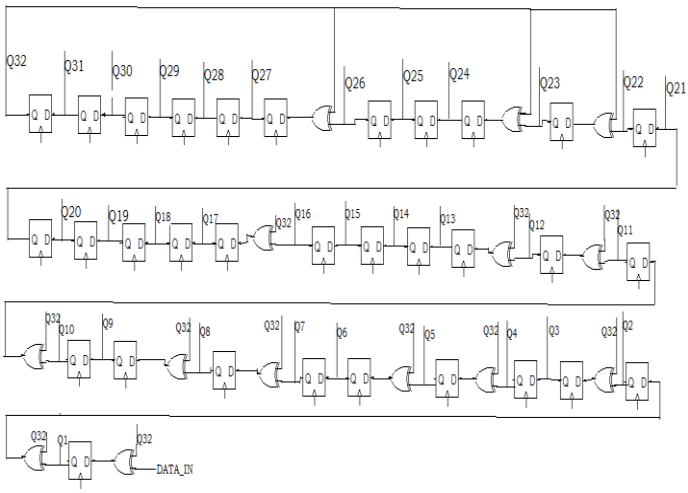

Fig-1: Proposed 32-bit CRC encoder and decoder

2.1 TSPC flip flop

The flip flop used in the proposed 32-bit CRC encoder and decoder architecture is the Split output concept based true single phase clock (TSPC) flip flop as shown in Figure (2).

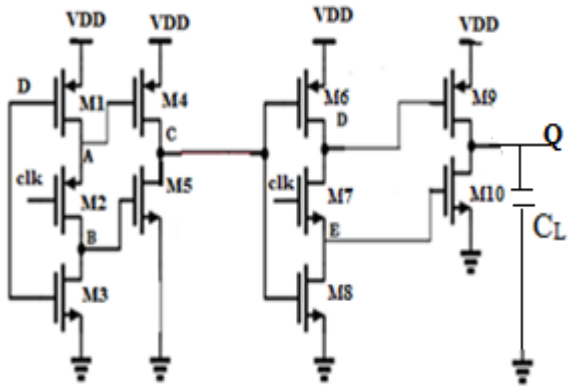

Fig- 2: Split output concept based true single phase clock (TSPC) flip flop

A simplified version of the true single phase clock latch stages is called split output latch. Only the first inverter is controlled by the clock resulting in clock load reduction by half and reduction of the number of transistor. TSPC flip flop can be modified for low power and less delay by cascading split output latches in which output of the first stage is split.

In submicron technologies, the Split output concept based true single phase clock (TSPC) flip flop can be used due to reduced threshold voltages. This modified TSPC flip flop results in elimination of clock skew which arises due to different clock phases.

2.2 XOR gate

In proposed 32-bit CRC encoder and decoder architecture feedback network is formed by BDD(binary decision diagram)based XOR gate which decreases power and delay as shown in Figure(4).

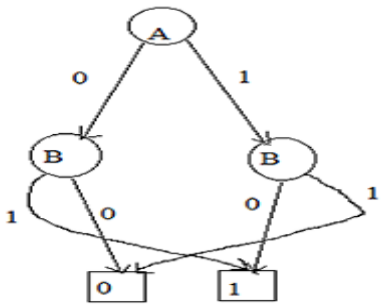

Fig- 3: Binary decision diagram of XOR gate

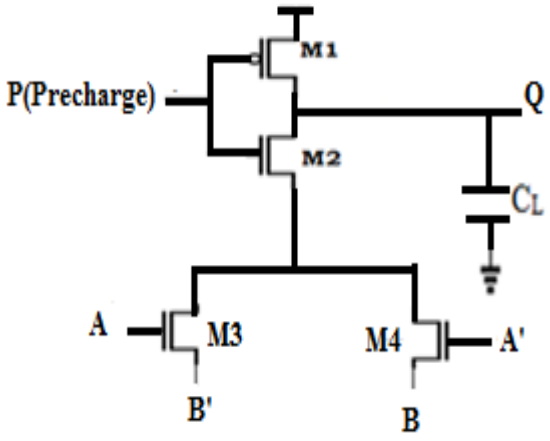

Fig- 4: BDD based XOR gate

Any Boolean function F(x_1, x_2, . . . , x_n) can be represented by a BDD, which is a Directed Acyclic Graph (DAG) with one root node and two leaf nodes labeled as 0 and 1.Binary decision diagram (BDD) is a useful and often compact representation mechanism for Boolean function that has application in logic synthesis, verification as well as in many problem outside the field of logic design.

BDD based XOR gate is an efficient design for power reduction. Some parts of the proposed XOR gate design are BDD-based which have been implemented using Pass Transistor Logic (PTL) with top pre-charge logic, we term it as dynamic PTL. This approach represents a novel application of BDD principles for XOR gate design for optimizing the transistor count and power dissipation.

3. DESIGN OF 32-BIT CRC ENCODER AND DECODER ARCHITECTURE

To drive a output capacitive load, Split output concept based true single phase clock (TSPC) flip flop and BDD based XOR gate circuits are designed by assuming total current flows through the circuit is 72µA and 18 µA and slew rate of 1.8v/µsec. Assuming supply voltage to be 1.8V, and using $\mu_n C_{ox}$=110µA/V^2 and $\mu_p C_{ox}$=30µA/V^2, the values of W/L of all transistors are calculated.

3.1 Design of split output concept based TSPC flip flop

1) First assume total current flow from power supply is 72 µA and current flowing from one branch of TSPC flip flop is 18 µA.

Slew rate=I_O/C_L..... (1)

Since I_O = 18 µA

$C_L = 10$ pF .....(2)

2) Power = V I

Power= 1.8v x 72 x10^{-6}

Power= 0.1296 mW .....(3)

3) Power dissipation = C_L* (V_{dd})^2* f

Frequency of operation, f = 4MHz .....(4)

4) The dimensions of M_9, M_{10} is obtained using,

$$I_{dp} = \frac{\mu_p C_{ox}}{2} (W/L)_P (V_{gs} - |V_{tp}|)^2$$

$$I_{dn} = \frac{\mu_n C_{ox}}{2} (W/L)_n [(V_{gs})_n - V_{tn}]^2$$

5) The dimensions of M_6, M_7,M_8 is obtained using,

$$V_M = \frac{V_{dd} - V_{tp} + V_{tn}\sqrt{\beta_n/\beta_p}}{1+\sqrt{\beta_n/\beta_p}} \quad \text{..... (5)}$$

Assume V_M = 0.7V and V_M (mid-point voltage) to be like that both NMOS & PMOS are in saturation

6) The dimensions of M_4, M_5 is obtained using ,

$$\frac{(W/L)_P}{(W/L)_n} = \frac{K_n V_{Dsat}(V_M - V_{tn} - V_{Dsat}/2)}{K_P V_{Dsat}(V_{dd} - V_M + V_{tp} + V_{Dsat}/2)} \quad \text{.....(6)}$$

Calculate V_{Dsat} and obtain $(V_{gs})_4$ and $(V_{gs})_5$ by using

$V_{Dsat} = (Vgs)_p - V_{tp}$

7) The dimensions of M_1, M_2, M_3, is obtained using ,

$$V_M = \frac{V_{dd} - V_{tp} + V_{tn}\sqrt{\beta_n/\beta_p}}{1+\sqrt{\beta_n/\beta_p}}$$

Assume V_M = 0.55V

Table-1: W/L Ratios of the Transistors of the split output concept based TSPC Flip-Flop:

Transistor	W/L ratio
M9	7.47µ/180nm
M10	575nm/180nm
M6	780nm/180nm
M7,M8	1 µ/180nm
M4	20 µ/180nm
M5	5.4 µ/180nm
M1	400nm/180nm
M2,M3	7.69µ/180nm

3.2 Design of BDD based XOR gate

1) First assume total current flow from power supply is 18 µA

Slew rate=I_O/C_L..... (7)

Since I_O = 18 µA

$C_L = 10$ pF .....(8)

2)The dimensions of M_1, M_2, M_3, M_4 is obtained using,

$$I_{dp} = \frac{\mu_p C_{ox}}{2} (W/L)_P (V_{gs} - |V_{tp}|)^2$$

$$I_{dn} = \frac{\mu_n C_{ox}}{2} (W/L)_n [(V_{gs})_n - V_{tn}]^2$$

Table-2: W/L Ratios of the Transistors of the BDD based XOR gate:

Transistor	W/L ratio
M1	1.5µ/180nm
M2	575nm/180nm
M3,M4	2.4µ/180nm

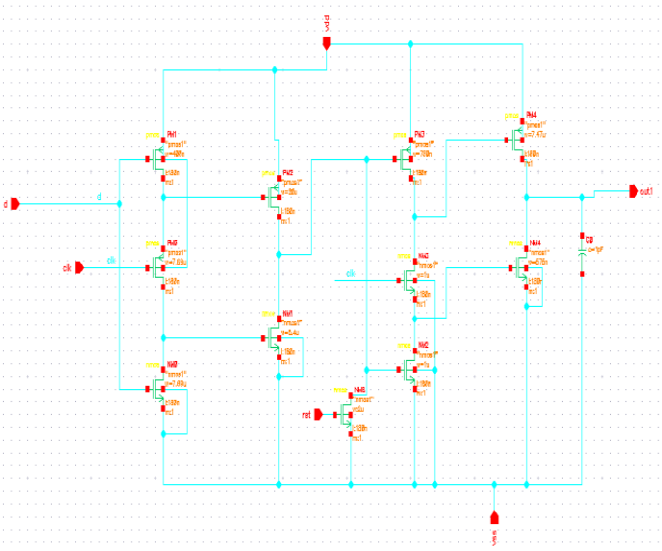

Fig-5: Schematic of split output concept based TSPC flip flop

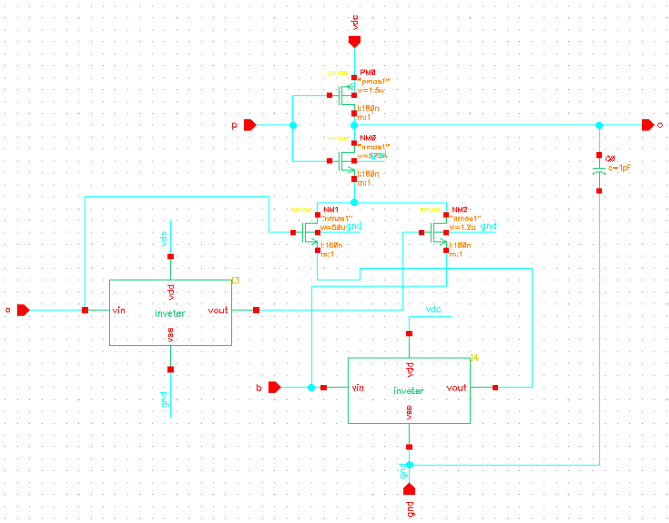

Fig-6: Schematic of BDD based XOR gate

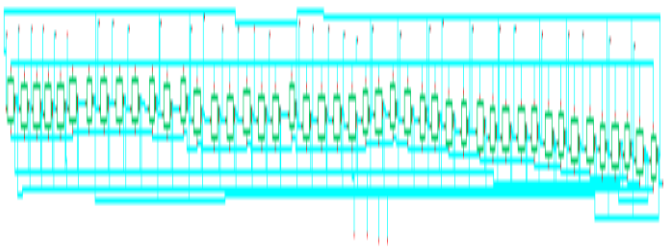

Fig-7: Schematic of proposed 32-bit CRC encoder and decoder

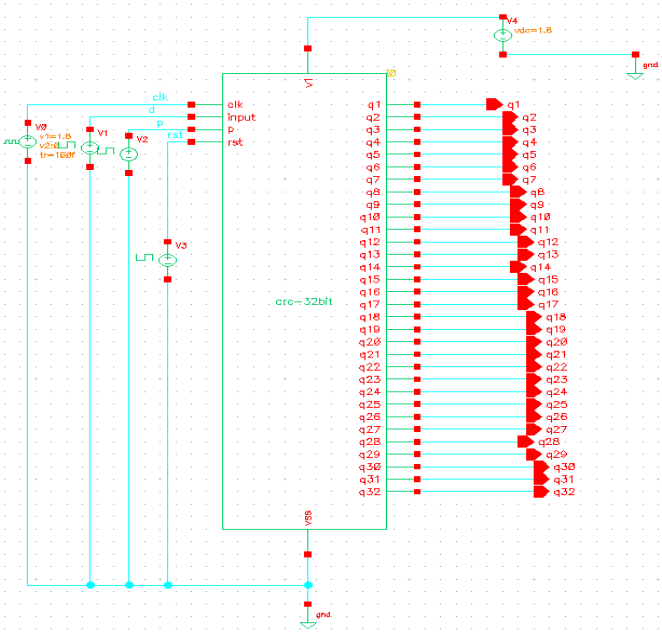

Fig-8: Test circuit of proposed 32-bit CRC encoder and decoder

4. SIMULATION RESULTS

Figure (9) shows the simulation result of split output concept based TSPC flip flop with power of 2.38µW and delay of 36.17ps.

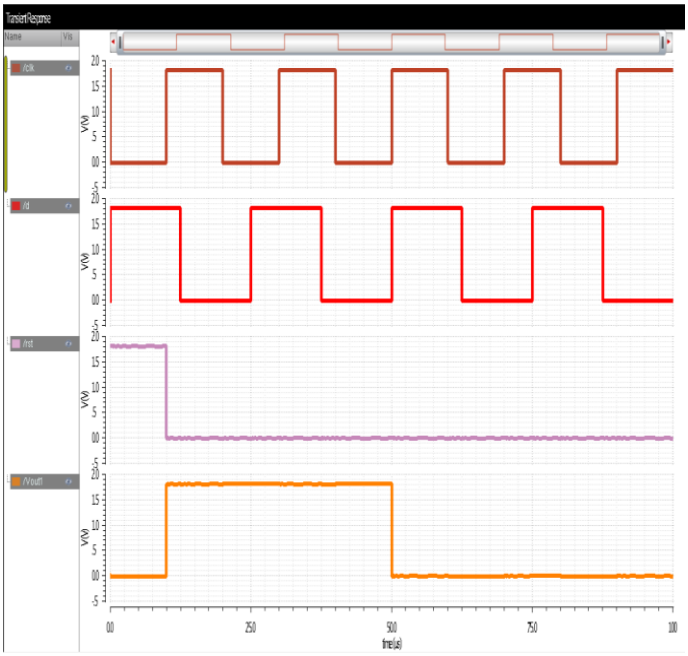

Fig-9: Simulation result of split output concept based TSPC flip flop

Figure (10) shows the simulation result of BDD based XOR gate with power of 705nW and delay of 17ps.

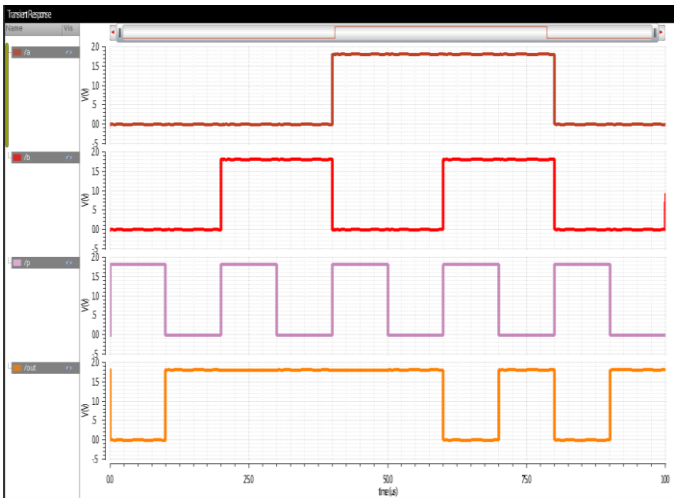

Fig-10: Simulation result of BDD based XOR gate

Figure (11) shows the simulation result of proposed 32-bit CRC encoder by assuming,

Data: 10110101101101011011 0101

Append 32 zeros at the end of data for 32 bit-CRC

Data: 10110101101101011011010100000000000000000000000000000000

Encoded data: 00011000011010101010101010001100

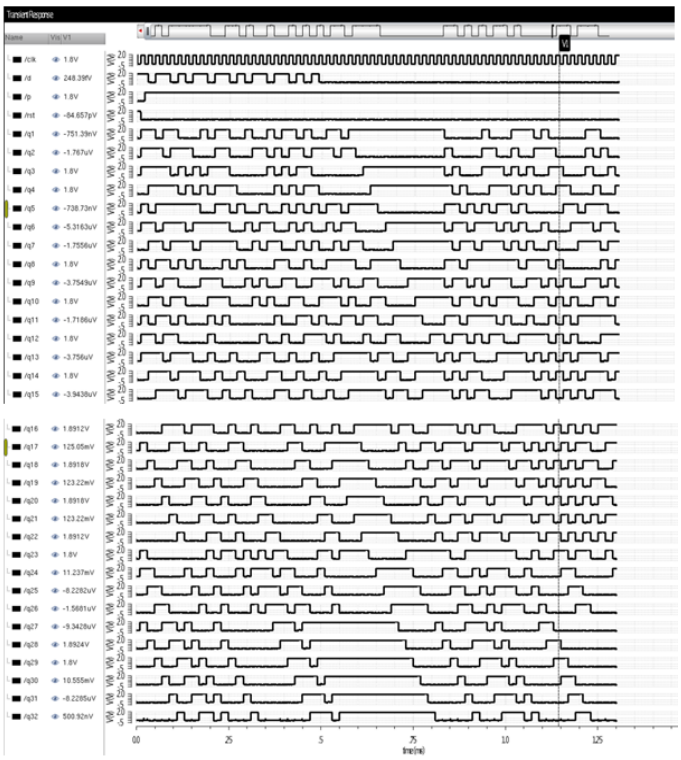

Fig-11: Simulation result of proposed 32-bit CRC encoder

Figure (12) shows the simulation result of proposed 32-bit CRC decoder.

Decoded data: 00000000000000000000000000000000

This means that data sent by the sender is assume to be correct and accepted by the receiver.

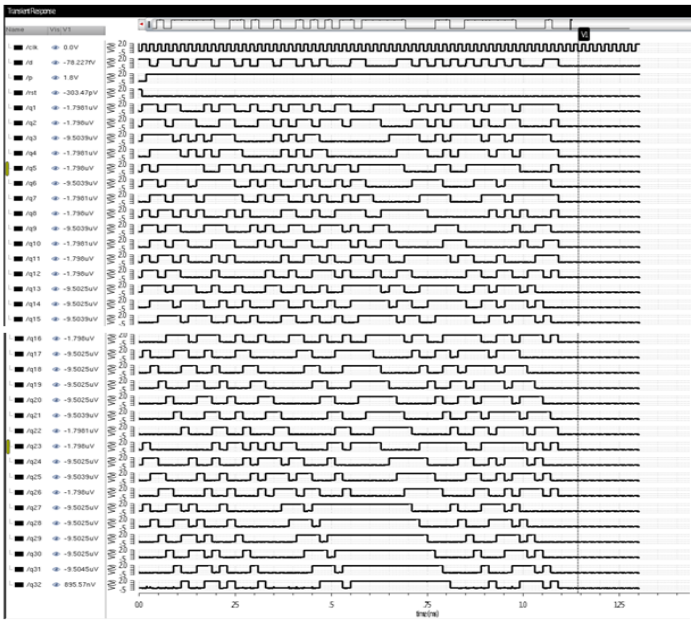

Fig-12: Simulation result of proposed 32-bit CRC decoder

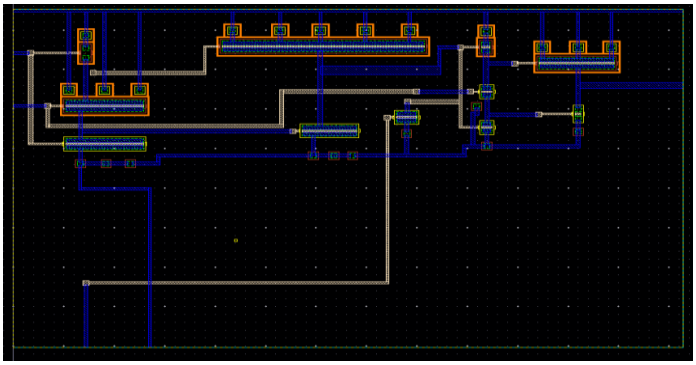

Fig-13: Layout of split output concept based TSPC flip flop

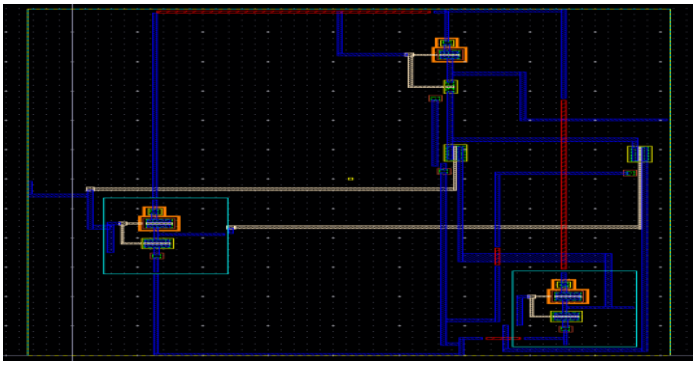

Fig-14: Layout of BDD based XOR gate

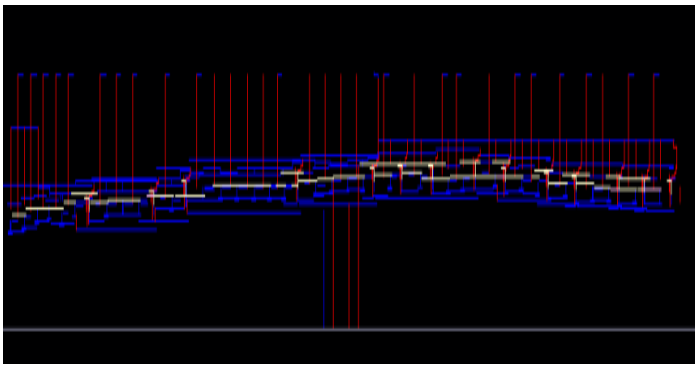

Fig-15: Layout of 32-bit CRC encoder and decoder

Table-3: Comparison between existing and proposed flip flop architecture [3]:

Flip flop design	Power(µW)	Delay
Conventional TG flip flop	9.38	10.13ns
C²MOS flip flop	9.95	10ns
Pass flip flop	5.60	138ps
Pass isolation flip flop	3.75	100.2ps
TSPC flip flop	3.458	37ps
Split output concept based TSPC flip flop	2.38	36.17ps

Table-4: Comparison between existing and proposed XOR gate architecture:

XOR gate Design	Power(nW)	Delay(psec)
CMOS XOR gate	1698	119
BDD based XOR gate	705	17

5. CONCLUSION

32-bit CRC encoder and decoder for Ethernet applications using LFSR (linear feedback shift register) has been designed and results are verified in terms of power and delay. Performance comparison of different flip flops and XOR gate for LFSR design are obtained in terms of power and delay. It is concluded that design of BDD (binary decision diagram) based XOR gate requires only 8 transistors which provide 58% improvement in power and also increases speed of computation. Above performance comparison shows that split output based TSPC flip flop architecture is having low power and less delay compared with conventional transmission gate based single edge triggered flip flop,C²MOS flip flop, pass flip flop and pass isolation flip flop. Layout of 32-bit CRC, modified split output based TSPC flip flop and BDD based X-OR gate has been done at cadence virtuoso at 180nm technology.

6. FUTURE WORK

For further improvement in speed and power parallel implementation of 32 bit CRC can be done at transistor level in cadence virtuoso at 180nm technology.

REFERENCES

[1] Elena Dubrova and Shohreh Sharif Mansouri," A BDD-Based Approach to Constructing LFSRs for Parallel CRC Encoding"IEEE 42nd International Symposium on Multiple-Valued Logic,pp.128-133,2012.

[2]. Shan Mary Cherian, Naveena S George, Sherin Mary Enosh ,Sunitha S Pillai,"An efficient way of generating CRC bit for serial data using any polynomial", International

Journal of Scientific and Research Publications, Volume 4, Issue 4, April 2014.

[3]. Imran Ahmed Khan, Mirza Tariq Beg," A New Area and Power Efficient Single Edge Triggered Flip-Flop Structure for Low Data Activity and High Frequency Applications", Innovative Systems Design and Engineerig, Vol.4, No.1, 2013.

[4]. Sameer Gull Alie, Ms.Tarana Afrin Chandel, Jehangir Rashid dar,"Power and delay optimized edge triggered flip flop for low power microcontrollers",International Journal of Scientific and Research Publications, Volume 4, Issue 5, May 2014 , ISSN 2250-3153.

[5]. W. Stallings, Data and Computer Communications. Prentice Hall, 2000. T. Ramabadran and S. Gaitonde, "A tutorial on CRC computations,"Micro, IEEE, vol. 8, pp. 62 – 75, aug. 1988. S. Golomb, Shift Register Sequences. Aegean Park Press, 1982.

[6]. S. B. Akers; "Binary decision diagrams", IEEE Trans. Computers, Vol. C-27(6) 1978, pp. 509-516.

[7]. E. Stavinov, "A practical parallel CRC generation method," Feature Article, pp. 38–45, Jan. 2010

[8] Xifan Tang , Jian Zhang , Pierre-Emmanuel Gaillardon , Giovanni De Micheli,"TSPC Flip-Flop Circuit Design with Three-Independent-Gate Silicon Nanowire FETs", Circuits and Systems (ISCAS), IEEE International Symposium on,pp.1660-1663,2014.

[9] J. McCluskey, "High speed calculation of cyclic redundancy codes," in Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays, FPGA '99, (New York, NY, USA), pp. 250–256, ACM, 1999.

[10]. M. Sprachmann, "Automatic generation of parallel CRC circuits," IEEE Des. Test, vol. 18, pp. 108–114, May 2001.G. Campobello, G. Patane, and M. Russo, "Parallel CRC realization,"Computers, IEEE Transactions on, vol. 52, pp. 1312 – 1319, oct. 2003.