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Estimation of Real Dynamic Power on Field Programmable Gate Array

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Abstract ***This paper presents register transfer level power models for field Programmable Gate Array. The development of the dynamic power models results from a real measurement bench based on Spartan6. Power models are in function of the activity rate and the precision. The results are compared with Xilinx Xpower tool. We have validated our operator's power models by using the FIR filter computing application in an FPGA Spartan6. The experimental results show that the average accuracy of the model is higher and the maximum reached average error is equal to 5.5%.***

1. Introduction and related works

The increase in the operating clock frequency and the integration density make full consideration to Field Programmable Gate Array (FPGA) power consumption. The embedded systems battery operating time and the circuit reliability are so much affected by the power dissipation increase. FPGA circuit presents the flexibility advantage which enable us to prototype several embedded applications, but its performance is affected by the higher consumption power. So, it is very interested to control power consumption and to develop accurate estimation methodologies and techniques. This work deals in this context. Many estimations approaches were applied at each conception level starting from physical level to system level. It is widely known that the greatest power gain can be achieved at high level.

High level estimation approaches can be divided into two categories: probabilistic and statistical. Probabilistic techniques [1], [2], [3] are based on input stream to estimate the switching activity of the circuit. Probabilities was first used in [4] where a zero delay was assumed and a temporal independence assumption was considered, so transition probabilities are computed using the signal probabilities which are supplied by the user at the inputs and propagated from the inputs to the outputs of the circuit. Another probabilistic method was developed in [5], [6] where the circuit activity transition density measure was used and the inputs were with spatial independence. These techniques are accurate but they can't estimate the glitches power. Power statistical techniques [7], [8], [9] used random input patterns and monitor the power dissipation by simulator. In order to establish accurate measure, high number of simulated vectors is required, which increase the estimation run time. A Monte Carlo simulation technique was studied in [10] to overcome this problem. This technique uses input vectors that are randomly generated. Survey sampling perspective was addressed in [11]. The sequence vectors were provided to estimate power dissipation of a given circuit with certain statistical constraints such as confidence level and error. This technique divides the vectors sequence into consecutive vectors, to constitute the population of the survey. The average power was estimated by simulating the circuit by a large number of samples drawn from the Population [12]. Otherwise, some power macro modeling techniques have been introduced in [13], [14]. In [15], the authors used analytical approach without considering temporal correlation only the spatial correlation was considered. Other register transfer level (RTL) power macro models tried to exploit the low level characteristics have been explored in [16], [17], [18], [19]. These models depend on the probability, the transition density, the spatial and temporal correlations taking into account the spatial independence between signals.

We present in this work an estimation power methodology based on using a real measurement bench using the Spartan 6 environment because the accurate estimates starts from real measures. The real power estimation was compared to Xilinx Xpower tool results. The methodology was applied to arithmetic operators such as adders and multiplier. The validation was performed in filters FIR applications.

This paper is organized as following. In the first part we introduce the problem and describe some related works. In the second one, we describe the dynamic power estimation methodology. The operator's power models are presented in the third part. The results are reported in the fourth part. Finally, we conclude and explore our future works.

2. Dynamic power estimation methodology

We have developed a power measurement bench based on the Attlys Board environment [20], using the FPGA Spartan6 LX45 (Technology 45nm). This device is dedicated to optimize the high performance logic. It allows us to better control the operating implemented application through USB2 system provided by Digilent Adept. We can also configure the FPGA and control in real-time the currents and the consumed powers of different parts including the core and the I/O powers. The developed models are obtained by using our real bench with varied input activity factor. All the inputs/outputs are registered and the applications are placed near the FPGA I/O to avoid additional routing power and to minimize the glitches power. The models are based on the input precision and the activity_rate at fixed frequency to 100MHz. The following figure describes the power estimation

methodology (Fig1.). A comparison was done between our methodology and the Xilinx Xpower tool.

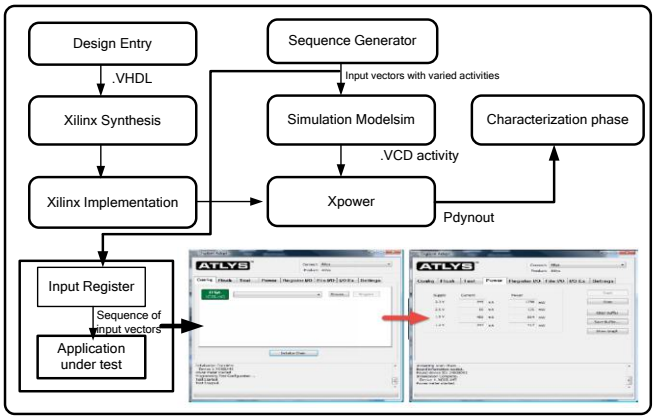

Fig1. Estimation methodology description

For each input sequence vectors, we calculate its activity_rate (activity_inputs) as the average number of transitions from 0→1 and 1→0 of each bit b_i of the vector l and then we propagate these sequences from the input to the output in order to evaluate the application activity _rate. The average activity (α) is calculated by the basic formula as follows:

$$average\_activity = \frac{1}{w} * \sum_{w} \left(\frac{1}{L-1} * \sum_{l=1}^{L} \left(tr_{bi(l)\rightarrow bi(l+1)}(0\rightarrow 1) + tr_{bi(l)\rightarrow bi(l+1)}(1\rightarrow 0) \right) \right)$$

(1)

Where L is the number of vectors sequence and w is the precision of each vector l; $1 \leq b_i \leq w$

This experimental bench allows as to:

- Measure the static power when no application is implemented in FPGA circuit.
- Measure the global power for different input precision and different activity rates.

The measure of different dynamic power is commanded by the two signals reset and start. We measure in first step the power consumed by the input vectors register. In the second step, the inputs are send to the application test (start='1' and reset='0'), we measure in this case the global consumed power and

$$P_{dyn\ global} = P_{dyn}(Register) + P_{dyn}(Application)$$

then deduce the application consumed power, also the different component of dynamic power such as (Pdyn(clock),Pdyn(signal), Pdyn(logic) and Pdyn(I/O)).

3. Basic Operator models

The static power is assumed to be invariant in function of the activity design because the implemented circuit that we have implemented is small and the static power increase is negligible. We reported in this part, the measured power by our tool and the Xpower tool.

3.1. Adder model

The table bellow (Table1) illustrates a comparison between the Xpower estimated power and the measured power while using our methodology for the 8 bit Adder arithmetic basic operators. The column one describes the activity variation from 25% to 100%. The total real measured power is outlined in the second column and its different power components (Pclock,Plogic, Psignal and PI/O), the column three reports the Xpower estimated power where as the last one describes the average error between the two methods. The last column rapports the error between the two measured powers. An average error of 54% outlines the inaccuracy of the Xpower tool as indicated in [21] and justifies the accuracy of our real measurement power tool

Tab1. Measured dynamic power of an adder (8 bit) on spartan6 at F=100MHz

α (%)	Pdyn(mw) Xpower					P dyn real	Error (%)
	clock	logic	signal	I/O	total		
0	1.83	0.0	0.0	0.0	1.83	0.84	54.0
25	1.83	1.62	6.67	3.9	14.02	6.23	55.5
50	1.83	4.005	12.80	8.86	27.5	12.9	52.8
100	1.83	7.009	18.41	19.96	47.2	21.2	55.0

The variation of the adder (8 bit) dynamic power and its components at frequency F=100MHz is described in the following figure (Fig2) and its analytical power model of the real measured power function to the activity_rate is mentioned in figure 3 and equation (2).

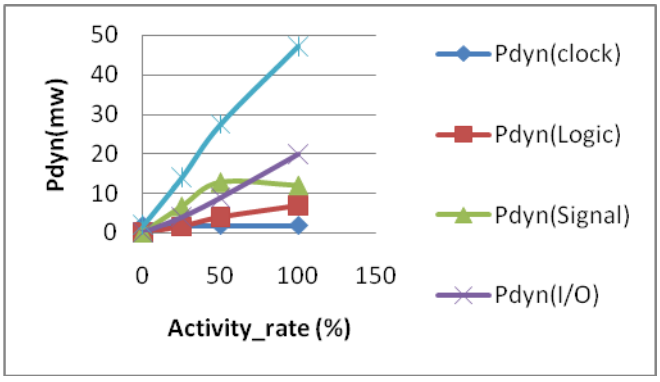

Fig2. Variation of the adder (8 bit) dynamic power and its components at F=100MHz

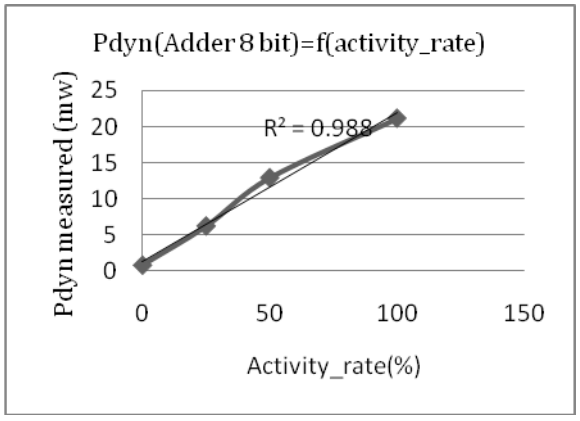

Fig3. Analytical model of the 8 bit adder in function of the activity_rate

$$Pdyn(Adder)(\alpha) = 0.204 \times \alpha + 1.366 \quad (2)$$

In order to expand the generic adder, we have varied the input precision from 8, 16, 32, 64 to 128 bits, we have measured the consumption dynamic power (Tab2). The figure2 describe the variation of dynamic power of the generic adder in function of the activity rate at fixed frequency to 100 MHz.

Tab2. Dynamic power of the generic adder with varied input precision (w) and activity_rate at frequency F=100MHz

W(bits)	Activity_rate(%)	Pdyn(measured) (mw)
8	0	0.84
16	25	14.5
32	50	41.65
64	100	88.98

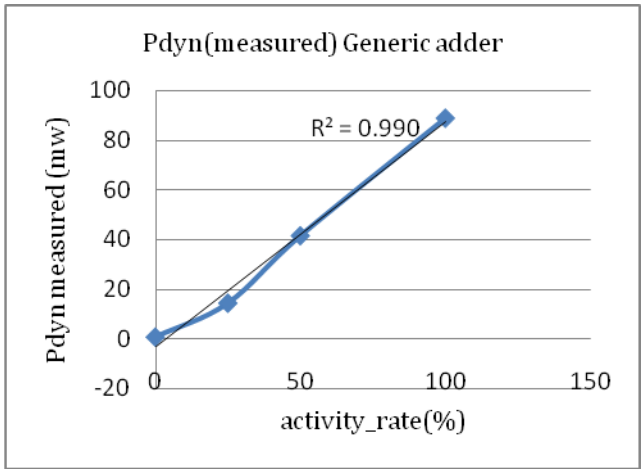

Fig4. Linear variation of the generic adder dynamic power in function of the activity_rate at F=100MHz

The variation of the dynamic power of the generic adder can be approximated by the linear model (Fig4) as described by equation (3) at fixed frequency to 100MHz:

$$Pdyn(Adder)(\alpha) = 0.906 \times \alpha - 3.162 \quad (3)$$

3.2. Based Luts multiplier power model

The same measurement was done for the based luts multiplier (8×8) bit. The table and the figure as follow describe the variation of total dynamic power and its component while varying the activity_rate. The estimated dynamic power using the Xpower tool is described in the second column. The third column rapports the measured dynamic power while using our experimental bench where as the last column deals with the error between the two measured powers. We outlined an average error of 33% between the two results.

Tab3. Measured dynamic power versus the estimated one using the Xilinx Xpower tool for the based lut multiplier (8×8) bit

α (%)	Pdyn(mw) Xpower					P dyn real	Error (%)
	clk	logic	signal	I/O	total		
0	2.16	0.0	0.0	0.0	2.16	1.8	16.6
25	2.16	5.44	5.68	15.5	28.78	14.65	49.0
50	2.16	10.89	7.21	22,58	42.84	26.47	38.2
75	2.16	13.52	9.77	34.53	59.98	43.65	27.2
100	2.16	20.25	14.11	41.29	77.78	51.52	33.7

In order to expand the generic multiplier, we have varied the input precision from 8, 16, 32, 64 bits; and then measured the consumption dynamic power. The figure5 describe the variation of dynamic power of the generic multiplier in function of the activity rate at fixed frequency to 100 MHz.

Tab4. Dynamic power of the generic multiplier at frequency F=100MHz

W(bits)	Activity_rate(%)	Pdyn(measured) (mw)
8	0	1.8
16	25	42.65
32	50	104.12
64	100	223.45

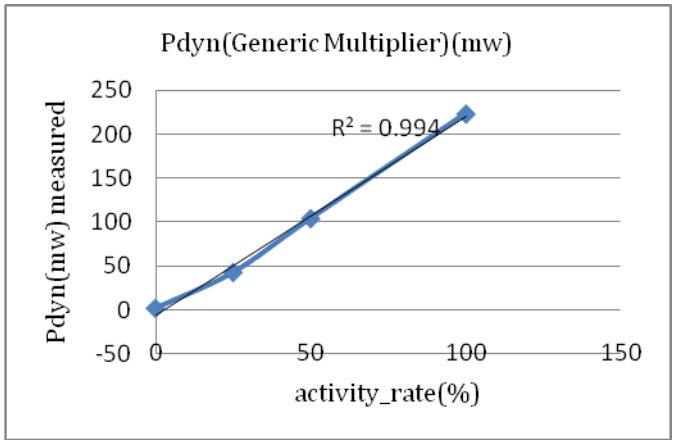

Fig5. Variation of the generic multiplier dynamic power in function of the activity rate at fixed frequency to 100MHz

The variation of the dynamic power of the generic multiplier can be approximated by the linear model (Fig5) as described by equation (4) at fixed frequency to 100MHz:

$$Pdyn(Multiplier)(\alpha) = 2.256 \times \alpha - 5.726 \quad (4)$$

4. Results

To validate the operator's power models, we have chosen two applications a FIR filter with 4 stages (a) and another with 20 stages (b). The FIR filter architecture is described by this figure (Fig6) and surface performances are reported in table5. The architecture is on pipeline, we have placed registers after every block made up of one multiplier and an adder in order to minimize the glitches power.

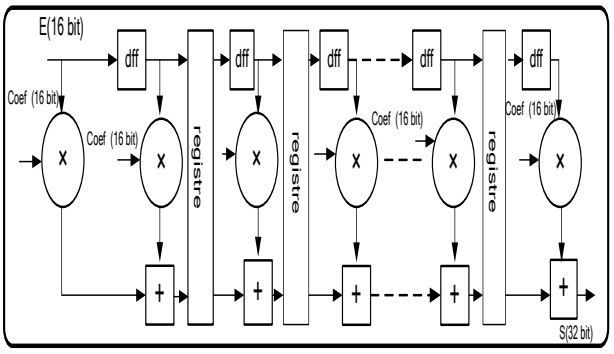

Fig6. Description of the FIR filter architecture

Tab5. The FIR filters surface performances

Architecture	Slices Luts	Slices Registers	IOBs	Occupation_rate (%)
FIR 4 stages	2310	1450	35	8.5
FIR 20 stages	8927	3875	35	33

Estimated dynamic powers are summarized in table 6 for FIR filters 4 and 20 stages. The column three rapports the Xpower dynamic power. The measured dynamic power obtained from our bench is described in the fourth column. The developed model for dynamic power issues of real measurement is mentioned in the fifth column where as the last one carried out the error between the real measured dynamic power and its corresponding model.

Tab6. FIR filters power consumption obtained from Xpower and real measures at fixed frequency to 100MHz

Architectures	α (%)	Pdyn(mw) Xpower	Pdyn real	Pdyn (model) (mw)	Error(%)
FIR 20 stages	25	702	354.23	368.89	3.97
	50	921	448.32	468.64	4.33
	75	1097	663.12	702.23	5.56
	100	1362	790.15	820.46	3.69
FIR 4 stages	25	175.23	87.23	91.46	4.62
	50	210.32	132.10	138.44	4.57
	75	276.42	174.85	181.24	3.52
	100	321.21	200.12	211.52	5.38

The table6 outlines an average error of 4.38% between the measured and estimated model which verifies the accuracy of our measurement methodology and our architectural power models.

5. Conclusion

We have presented in this paper a real power measurement methodology based on Spartan6. Some analytical power models for adders and multipliers were developed function of the activity rate at fixed frequency. A comparison was established between our results and there from Xilinx Xpower tool. We have validated our models and approach on a 4 and 20 stages FIR filters. We outline an average error of 4.38% between the measured and estimated model which verifies the accuracy of our measurement methodology and our architectural power models. As future work, we think to enhance our applications library and develop others power models at system level.

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BIOGRAPHIES

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