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A Systematic Design Approach for Low-Power 3-Bit 1 MS/s, 5v MDAC for Pipeline ADC and Design of 6 Bit Pipeline ADC using 3-Bit MDAC

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Abstract – ***The purpose of this work is to design a 3 bit MDAC for a pipeline ADC in a 0.25-µm CMOS technology. The ADC is designed according to thermometer coding. The latched comparator is used to reduce the power consumption. The MDAC designed in this paper is having the sampling frequency of 1Ms/s with the power consumption of mw. The 3-bit MDAC design is having the supply voltage of 5v and the gain of the differential amplifier is 8. The ADC output and power consumption are represented in the results. Finally the power dissipation of 6 bit pipeline ADC is concluded***.

Key Words: Analog-to-digital converter (ADC), Digital-to-Analog converter (DAC), Pipeline ADC, Multiplying DAC (MDAC).

1. Introduction

High performance and low power consumption ADCs are generally required in the communication systems and image processing systems. For these systems the power consumption of analog signal to digital should be low. According to the requirement different ADCs are designed. There are three main categories [10] to design the ADC:

1. Low-to-medium speed & high accuracy.
2. Medium speed & medium accuracy.
3. High speed & low-to-medium accuracy.

Integrating and sigma-delta ADCs are the low-to-medium speed & high accuracy ADC. In integrating type ADC the time required for the analog input voltage to exceed the reference voltage is proportional to the input voltage. The integrating ADC requires 2^N clock cycles to obtain N bits of resolution. Higher the resolution more the integrating time is required. Therefore as the accuracy of these ADC increases the conversion speed decreases.

Successive-approximation register (SAR) ADC is the type of medium speed and medium accuracy. SAR ADCs uses a comparator to successively narrow a range that contains the input voltage. At each successive step, the converter compares the input voltage to the output of an internal digital to analog converter which might represent the midpoint of a selected voltage range. The main disadvantage of SAR is that for higher resolution SAR ADCs become slower.

Flash converters are extremely fast compared to many other types of ADCs with high accuracy over a series of stages. But a Flash converter requires a huge number of comparators as compared to other ADCs. In this paper 3-bit MDAC design is presented with the supply voltage of 5v. Later a 6 bit pipeline ADC is designed with this 3 bit MDAC.

1.1 Pipeline ADC

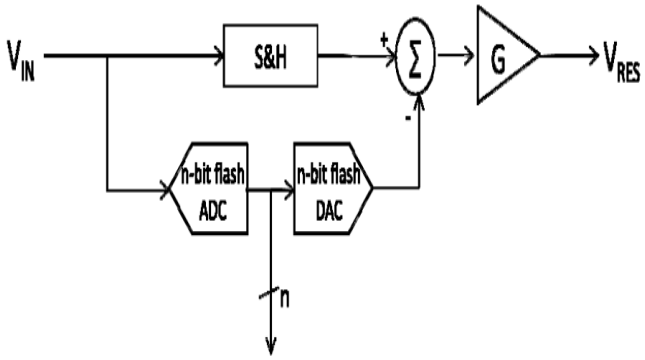

Figure 1 shows the pipeline ADC [8] each stage block diagram [4]. In each stage there is a sample and hold (S&H) block, a sub digital-to-analog (sub-DAC), a sub-ADC which is a flash type ADC [3], a subtractor and an inter-stage gain amplifier [5]. The sampled and hold takes the samples and apply to the sub-ADC which produces the output for this stage. The sub-ADC is a type of flash ADC. An n-bit flash ADC quantizes the analog voltage and produces the output in digital n bits. The digital output is then applied through an n-bit flash DAC to be re-converted into an analog signal. The summation node presented in the above diagram takes the input voltage from the sample-and-hold circuit and subtracts the DAC voltage from it. This difference voltage is then fed through a gain stage with gain G to produce the residue voltage, the output voltage of this stage. In a typical pipelined ADC implementation, the sample-and-hold circuit and flash

DAC are typically implemented in a single switched-capacitor circuit called a multiplying DAC, or MDAC. The amplification of the residue usually occurs with a closed-loop operational amplifier, usually consisting of a differential input, gain stage, bias circuitry, and a differential output stage. The residue voltage, VRES, becomes the input voltage to the next stage.

2. MDAC Design:

The first block of MDAC is sample and hold circuit. In S&H circuit the Pmos and Nmos are used. At the input of sample and hold circuit a clock box is used. The clock box is used to get balance clock at the output. As Nmos and Pmos are used in sample and hold circuit; to get balance output clock box is used. In ADC circuit the series resistors are used to generate the binary output. The resistors used are of 5K. These are applied to the opamp.

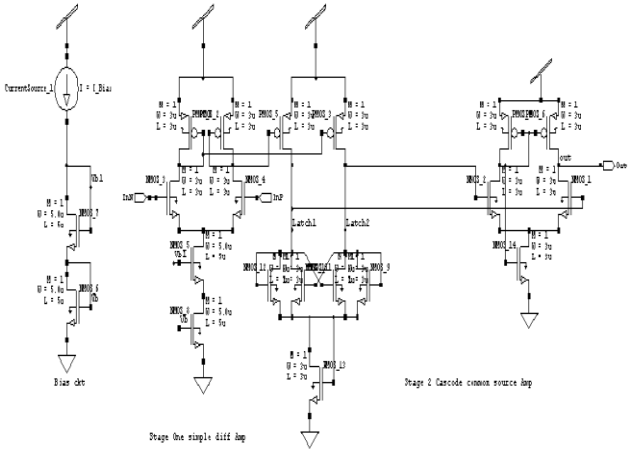

Figure 2: Latched comparator

The opamp act as a comparator. The comparator output is the thermometer coding. The code generated by converter is applied to the EX-OR gate which gives the binary output. This output is then connected to the NOR gate to produce 3 bit output. The EX-OR gate use the thermometer coding [7] to generate the desired output from circuit. The capacitors are used to reduce the kick back effect. The ADC used in this design is a simple 3 bit flash ADC. The output of ADC is converted into analog signal with the help of DAC to obtain the residue voltage. To obtain this voltage the R-2R ladder circuit is designed. Here before the R-2R circuit inverter is used because the output bits of ADC are opposite due to the use of universal NOR gate. The value of R is 100k and the value of 2R is 200k. The last stage of MDAC is the differential stage output or gain stage. The gain of this amplifier is 8. The input for the differential amplifier is one analog signal from the input and other from the DAC which is the residue voltage. Figure 2 shows the latch comparator which is used in ADCs. The latch comparator are uses the positive feedback to accomplish the comparison of two signals. Normally the latch has two modes of operation. The first mode disables the positive feedback and applies the input signal. The second mode enables the latch, therefore one value goes high and other will go low. A two phase clock is used to determine the mode of operation. Figure 3 shows the complete schematic of the MDAC.

3. Results:

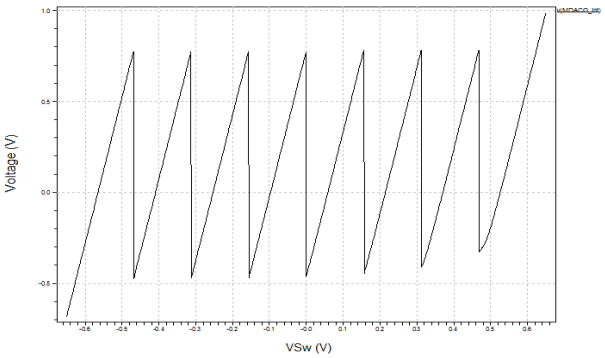

Figure 5: Residue output voltage from MDAC.

Figure 3 shows the residue output voltage from MDAC. The residue represents the amplified remainder from the subtraction of the DAC output voltage from the stage input voltage. The residue is swept from -1 to +1. For the generalized pipeline ADC described previously, each stage is responsible for quantizing n bits of the input sample.

Sr. No.	Parameter	6 bit pipeline ADC
1	CMOS process	250 nm
2	MDAC	3 bit
3	Power	Less than 7mw
4	Applied voltage	5v
5	Speed	1Ms/s

Table-I.Input parameters and result of 6 bit pipeline ADC.

Table I shows the power consumption by the 6 bit ADC. As shown in figure the power consumption by the 6 bit ADC is less than 7 mw.

4. CONCLUSIONS

In this paper a method for design knowledge on design of 3-bit MDAC has been developed. A 6 bit pipeline ADC is designed using 3-bit MDAC. The power consumption of the MDAC is less than 7 mw. From the simulation results it can be concluded that the final ADC output consists of a weighted sum of each stage's digital decision which is having less power consumption. The weightings are determined by the interstage gain or the gains of the residue amplifiers within each stage. The MDAC can be improved for high speed as it has less power consumption.

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