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Modeling and digital control of a synchronous buck converter for variable frequency operation

Kotha.Ayyappa[1],P.Deepak Reddy[2]

[1] *PG Scholar Department of EEE, Lakireddy Balireddy College of Engineering, Vijayawada, India*
[2] *Asst. Professor Department of EEE, Lakireddy Balireddy College of Engineering, Vijayawada, India*

ABSTARCT*: This paper explains the DC-DC converters operated at variable switching frequency for small signal averaged models. Mainly this paper proposed for synchronous buck converter should be operated at variable switching frequency. It can be done by considering on time and off time the switching period separately. For the design of digital feedback controller this modeling of converter is useful. This design gives the reliable converter dynamic operation. In this paper a multi loop PID controller architecture is designed and this design is based on the loop shaping of the proposed frequency domain transfer function. By using this variable frequency method tight output voltage regulation and dynamic performance achieved.*

***Keywords*:** *DC-DC converter, digital control, variable frequency operation, state space averaging.*

I.INTRODUCTION

Generally two control objectives are considered during controlling of DC-DC converters, they are performance and efficiency. The efficiency can be achieved by the controlling scheme operated at constant on time and constant off time at different load conditions [1-2]. And performance will be achieved by comparing the converters operated at different controlling laws. Basically the DC-DC converters are inherently variable control structures. A sliding mode control (SMC) technique is the one of the analog controlling technique[3-4]. This is based on the large signal representation of the circuit and it has a simple design procedure. Nowadays the digital controlling techniques will be more used in the implementation of the converter operation. So with the limited resolution and bandwidth technique of the digital control methods the analog control techniques are weakened. The time optimal control(TOC) technique is the one of the digital control method, in this a non linear interrupt based logic is added in parallel to the linear feedback loop to give optimal response[5-6].

In contrast to commonly used state space averaging (SSA)[7],[8] technique a generalized state space averaging technique is developed for the synchronous buck converter. In this paper linearized small signal representations of the circuit is derived and the on time and off time of the pulse width signal are taken as control inputs. By this way the converter could be operated at dynamic performance. The independent control system was designed and the multiloop PID [10] controller is based on the loop shaping of the frequency domain transfer functions(TF's).The variable frequency operation should be done by taking on time and off time of the pulse width modulated signal. The on time and off time are modulated by controller. Earlier the switching frequency taken as the controlling input but in this paper both on time and off time of the switching period are taken for the generalized approach. Thus constant on time, constant off time and variable on time, variable off time can be studied.In this proposed converter the parasitic equivalent series inductor (ESL) of the output capacitor is taken[11]. And it is more useful for the converter operated at point of load load (POL) applications.

2. CONVERTER MODELING

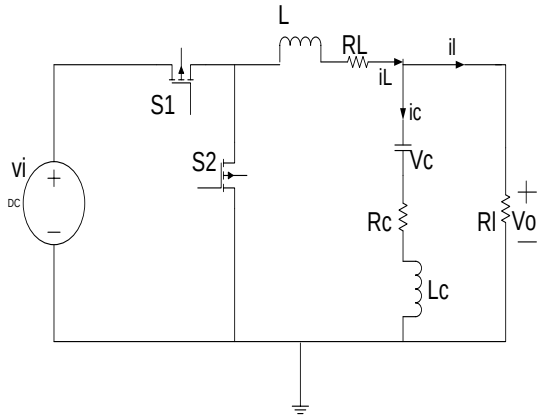

Fig. 1 synchronous buck converter

In this chapter the proposed converter should be modeled based on the small signal averaged and linearized technique. Based on this technique the on time $\widehat{t_{on}}$ and off time $\widehat{t_{off}}$ of the pulse width modulated signal are taken as additional control inputs. In the earlier averaging techniques only duty cycle is taken as control input. In this proposed synchronous buck converter shown in fig 1 the diode which was in conventional model will be replaced by switch. So this converter having two switches and their name given as high side switch S_1 and low side switch S_2.

When the converter is in on time condition S1 is on and S_2 is off and in off time S_1 is off and S_2 is on. The duty cycle (D) is given by

$$D = \frac{T_{on}}{T_{sw}} = \frac{T_{on}}{T_{on}+T_{off}} \quad \text{And}$$

$$D' = 1 - D \tag{1}$$

The duty cycle can be varied by two methods, they are first one is variation of on time when T_{sw} considered as constant and second one is variation of switching period.

$$d(t) = \frac{t_{on}(t)}{t_{on}(t)+t_{off}(t)} \tag{2}$$

The state space models are consider here are

$$\frac{dx(t)}{dt} = Ax(t) + Bu(t) \tag{3}$$

$$y(t) = Cx(t) + Du(t) \tag{4}$$

Where x , u , y are represented as states, inputs and outputs of the system and A ,B , C and D are represented as dynamic , input , output and direct transition matrices respectively.

By using equations (2),(3),(4) the derivation of the model should be more linearized and for the switching condition the on time and off time are taken as i=1 and i= 2 respectively. By using the above conditions the averaged model is more generalized.

The state space equations are representing the averaged system is given by

$$\frac{dx}{dt} = ((A1 - A2)\frac{t_{on}}{t_{on}+t_{off}} + A2)\,x + ((B1 - B2)\frac{t_{on}}{t_{on}+t_{off}} + B2)\,u \tag{5}$$

$$y = \left((C1 - C2)\frac{t_{on}}{t_{on}+t_{off}} + C2\right)x + \left((D1 - D2)\frac{t_{on}}{t_{on}+t_{off}} + D2\right)u \tag{6}$$

At the equilibrium point we have to consider small perturbations, the state X, input variable U , t_{on} and t_{off} are given by

$$x = X + \hat{x} \qquad u = U + \hat{u}$$

$$t_{on} = T_{on} + \widehat{t_{on}}$$

After substitute the above small perturbed values into state space model which earlier derived eq (5) and collecting DC terms

$$0 = Ax + \tilde{B}u$$

$$Y = Cx + \tilde{D}u \tag{7}$$

The averaged matrices are

$$A = DA_1 + D'A_2 \quad \tilde{B} = DB_1 + D'B_2$$

$$C = DC_1 + D'C_2 \quad \tilde{D} = DD_1 + D'D_2 \tag{8}$$

Collecting the AC terms and linearizes the model by neglecting second order terms yield the state space model is

$$\frac{d\hat{x}}{dt} = A\hat{x}(t) + \tilde{B}\hat{u} + bt_{on}\hat{t}_{on} + bt_{off}\hat{t}_{off}$$

$$\hat{y}(t) = C\hat{x}(t) + \tilde{D}\hat{u} + dt_{on}\hat{t}_{on} + dt_{off}\hat{t}_{off} \tag{9}$$

The column vectors b_{ton} , b_{toff} , d_{ton} , d_{toff} relating the new inputs $\hat{t}_{on}$ and $\hat{t}_{off}$ to the states and outputs respectively are found by linearizing and collecting AC terms and reordering the equations

$$\mathbf{b}_{ton} = (A_1X+B_1U)/(T_{on}+T_{off}) \tag{10}$$

$$\mathbf{b}_{toff} = (A_2X+B_2U)/(T_{on}+T_{off}) \tag{11}$$

$\mathbf{d}_{ton}= (C_1X+D_1U-Y)/(T_{on}+T_{off})$ (12)

$\mathbf{d}_{toff}= (C_2X+D_2U-Y)/ (T_{on}+T_{off})$ (13)

the resulting input and direct transition matrices are given by

$\mathbf{B}=[\tilde{B}\quad b_{ton}\quad b_{toff}]$ (14)

$\mathbf{D}=[\tilde{D}\quad d_{ton}\quad d_{toff}]$ (15)

Accordingly the state and output equation of the small signal model is

$$\frac{d\hat{x}}{dt} = A\hat{x}(t) + B\begin{bmatrix}\hat{u}(t)\\ \hat{t}_{on}(t)\\ \hat{t}_{off}(t)\end{bmatrix}$$

$$\hat{y}(t) = C\hat{x}(t) + D\begin{bmatrix}\hat{u}(t)\\ \hat{t}_{on}(t)\\ \hat{t}_{off}(t)\end{bmatrix} \quad (16)$$

The quantities $\hat{x}(t),\hat{y}(t),\hat{u}(t)$, $\hat{t}_{on}(t),\hat{t}_{off}(t)$ are the small AC variations around the equilibrium solution. The derived model treats the on time and off time of the switching period separately. And finally the derived model is enhanced model of the conventional model. And it is denoted as ESSA model.

The derived model can be applied to various DC-DC converters like buck, boost, buck boost, cuk etc. the model will be given in detail for synchronous buck converter for POL applications.

2.1 The proposed ESSA model for synchr-onous buck converter

The derivation is basically derived on large signal representation for the separate switching condition. The converter should be operated in on time and off time, the relevant switching operations are taken. When the converter is in on time condition the S_1 is on and S_2 is off then the system is given by

$$A_1=\begin{bmatrix}0 & 0 & \frac{1}{C}\\ 0 & -\frac{R_L+R_{on}+R_l}{L} & \frac{R_l}{L}\\ -\frac{1}{L_c} & \frac{R_l}{L_c} & -\frac{R_c+R_l}{L_c}\end{bmatrix}$$

$$B_1=\begin{bmatrix}0\\ \frac{1}{L}\\ 0\end{bmatrix}$$

$$C_1= [0 \quad R_l \quad -R_l]$$

$$D_1 = 0 \quad (17)$$

The state vector $X=\begin{bmatrix}v_c\\ i_L\\ i_c\end{bmatrix}$

Where v_c denotes the output capacitor voltage , i_L denotes the current through the output inductor and i_c denotes the current through the output capacitor. Here we have to consider $R_{on}+R_L+R_l=R_s$. In this modeling the capacitor current also taken as state variable because the ESL of the capacitor is considered. When the converter is conducted in off time means the S_1 high side switch is open and S_2 low side switch is close then the system is given by

$A_2=A_1$

$$B_2=\begin{bmatrix}0\\ 0\\ 0\end{bmatrix}$$

$C_2=C_1$ and $D_2 =0$ (18)

From equation (10) to (13)

$$b_{ton}=\begin{bmatrix}0\\ \frac{D'v_i}{L(T_{on}+T_{off})}\\ 0\end{bmatrix} \quad b_{toff}=\begin{bmatrix}0\\ -\frac{Dv_i}{L(T_{on}+T_{off})}\\ 0\end{bmatrix}$$

And $d_{ton}=d_{toff}=0$ (19)

From this modeling of the converter the input to output transfer function relation gives

$$\hat{v}_o = G_s(s)\begin{bmatrix}\hat{v}_i\\ \hat{t}_{on}\\ \hat{t}_{off}\end{bmatrix} \quad (20)$$

Then the transfer matrix is given by

$$G_s(s) = C(sI - A)^{'}B + D =$$

$$(1/(LL_cS^3 + (L(R_c + R_l) + L_cR_s)$$

$$+(L+(R_cR_s+R_l(R_{on}+R_L)))Cs+R_s)*$$

$$\begin{bmatrix} DR_l(L_cCs^2+R_cCs+1) \\ D'v_i\frac{R_l(L_cCS^2+R_cCs+1)}{T_{on}+T_{off}} \\ -Dv_i\frac{R_l(L_cCS^2+R_cCs+1)}{T_{on}+T_{off}} \end{bmatrix}^T \quad (21)$$

From the equations (20),(21) the on time control transfer function and off time control transfer function should be derived.

III. CONTROLLING DESIGN PROCEDURE

In this proposed model there are two controlling inputs i.e. $\hat{t}_{on}$ and $\hat{t}_{off}$. The transfer matrix derived in eq. (21) indicates small signal response of the output voltage $\hat{v}_o$ to the changes with these controlling signals. The converter switches are triggered by DPWM to which the on time and off time of the period can be separately given. The on time and off time control transfer functions can be derived by using eq. (20) and (21). From which on time $\hat{t}_{on}$ to the output voltage $\hat{v}_o$ is given as $G_{s,t_{on}}(s)=G_s[2]$ and the off time $\hat{t}_{off}$ to the output voltage $\hat{v}_o$ is given as $G_{s,t_{on}}(s)=G_s[3]$. The symbol $G_s[i]$ denotes the i^{th} column of the $G_s[S]$.

For this multi loop PID method the feedback loops will be tuned separately by using control to output transfer functions given in eq. (20)

Table 1.Parameters of the converter

Parameter	value
Input voltage	12V
Inductance	320nH
Capacitance	660uF
Switching frequency	780kHz
R_L	1m ohm
R_C	1m ohm
R_{on}	15m ohm
L_C	1 nH

The above tabulated parameter values are useful for the POL applications in the industry system.

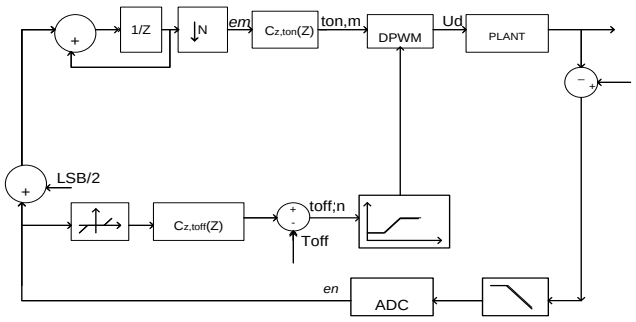

Fig-2: Structure of the PID controller

III.A. On time control design

The on time control design is based on the open loop transfer function of the model derived in the eq. (21). The control structure for the converter shown in fig 2. In the figure the digital output voltage error signal e_n is fed to the digital averaging and down sampling filter. The filtering stage used for the two purposes, first one is it ensure accurate dc value of the output voltage error signal from subsequent and 2nd one is reduction of sampling rate. The control input at the low rate e_m computes as

$$e_m = ((V_{ref} - v_{o,n}) + (V_{ref} - v_{o,n-1}) + \dots (V_{ref} - v_{o,n-N+1}))/N$$

where N is the number of samples considered and V_{ref} is the targeted DC voltage.

With a PID control law $C_{z,ton}(Z)$ the on time $t_{on,m}$ of the pulse width modulated signal for the next switching cycle can be computed, the digital controller design procedure can be done in q-domain, where mainly the same design procedure can used in s-domain. The discrete time TFcan be transformed to q-domain by applying bilinear transformation[12],[13].

$$G_{z,t_{on}}(Z) = \frac{z-1}{z} Z\left\{\frac{G_{s,t_{on}}(s)}{S}\right\}$$

$$G_{q,t_{on}}(q) = G_{z,t_{on}}\left(z = \frac{1 + \frac{q}{\Omega_{0,t_{on}}}}{1 - \frac{q}{\Omega_{0,t_{on}}}}\right)$$

Where $\Omega_{0,t_{on}} = \frac{2}{T_{sw}}$ and

$$\Omega = \Omega_{0,t_{on}} \tan\left(\frac{\omega}{\Omega_{0,t_{on}}}\right)$$

Where $G_{s,t_{on}}(s)=G_s[2]$ is derived in eq. (21) as the transfer function relating the input $\hat{t}_{on}$ to the output voltage $\hat{v}_o$ when $\hat{v}_i = 0$ and $\hat{t}_{off}=0$. And Z{X(s)} is given by $Z\{(L^{-1}\{X(s)\})$ at $t=kT_s$. The starting point for the controller design task is open loop TF

$$G_{q,sys,t_{on}}(q) = G_{q,t_{on}}(q).G_{q,lp}(q).e^{\frac{-qT_{on}}{2}}$$

In which $G_{q,lp}(q)=\frac{1}{\frac{q}{2\pi f_{lp}}+1}$ models the first order analog low pass filter and $e^{\frac{-qT_{on}}{2}}$ is the delay of the DPWM on the on time is approximated by design task of third order pade approximation. The on time control loop is dominant during steady state operation and it remove any steady state error. The q-domain controller TF can be transformed to z-domain by applying the trapezoid approximation

$$C_{z,t_{on}}(z) = C_{q,t_{on}}\left(q = \frac{2}{T_{sw}}\frac{z-1}{z+1}\right)$$

$$=5.43*e\text{-}6\frac{(z-0.92)(z-0.85)}{(z-1)(Z+0.017)}$$ for the sampling frequency f_{sw}=780kHz. The output of the on time $t_{on,m}$ is saturated before it is passed to the DPWM block. The lower and upper limits should be 2% and 20% of the nominal switching period.

III.B. Off time control design

The off time control loop takes the error samples delivered by ADC and it passed to the off time control law. In this proposed off time control design a non linear mapping (dead zone) has been added. Because the off time control loop reacts only when certain threshold output voltage error is exceeded. This non linear mapping used to boost the response of the off time loop. The dead zone has been set to ±2 ADC quantization levels. The gain of the off time control loop has been computed based on the open loop TF

$$G_{z,t_{off}}(Z) = \frac{z-1}{z} Z\left\{\frac{G_{s,t_{off}}(s)}{S}\right\}$$

$$G_{q,t_{off}}(q) = G_{z,t_{off}}\left(z = \frac{1 + \frac{q}{\Omega_{0,t_{off}}}}{1 - \frac{q}{\Omega_{0,t_{off}}}}\right)$$

Where $\Omega_{0,t_{off}} = \frac{2}{T_{ADC}}$ and

$$\Omega = \Omega_{0,t_{off}} \tan\left(\frac{\omega}{\Omega_{0,t_{off}}}\right)$$

Where $G_{s,t_{off}}(s)=G_s[3]$ is derived in eq. (21) as the TF relating the input $\hat{t}_{off}$ to the output voltage $\hat{v}_o$ when $\hat{v}_i = 0$ and $\hat{t}_{on}=0$. The open loop TF is given by

$$G_{q,sys,t_{off}}(q) = G_{q,t_{off}}(q).G_{q,lp}(q).e^{q\left(\frac{T_{off}}{2}-T_{ADC}\right)}$$

Thus the feedback gain is given by

$$C_{z,t_{off}}(z) = -k_p = -1.044 * e - 5$$

III.C. DPWM design

The dpwm block is plays a main role in this presented control structure. Which combines the both on time $t_{on,m}$ and off time $t_{off,n}$ of each period. So generated switching function, the DPWM design is very careful to design. The on time is updated once per switching period where as the off time is updated at the rate of ADC. The switching period is started and the signal is being generated with logic high 'H' and logic low 'L'. The quantizer block is designed with the quantizer value is $1/2^n$. where n is the no of bits are taken. And the saturated block is designed with the duty cycle value is minimum and maximum for lower and upper limits respectively.

III.D. ADC design

The error voltage value gained is in analog mode which is converted to digital by using ADC block. The ADC converter is designed with 4 bit resolution over 2v (-1v to +1v) quantization step v_q=0.125v and resolution is 4 bits. So the quantization interval is $2/2^4$. In this present

proposed model ESL of the output capacitor is used, because of this in combination with short on phases and large current magnitudes, a significant spike like ripple appears in the output voltage . So for this ripples can be disappear with first order low pass filter is designed. And it is placed at the input to the ADC. The cut-off frequency of low pass filter is 3MHz.

IV. SIMULATION RESULTS

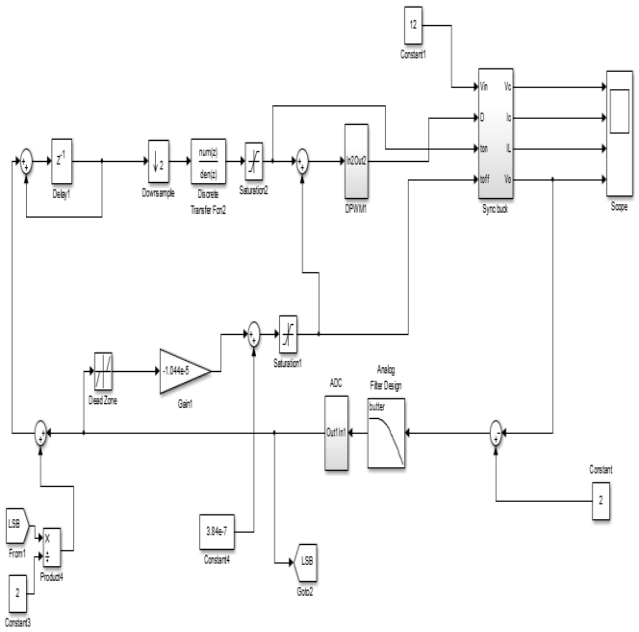

Fig-3.simulink block diagram for control architecture

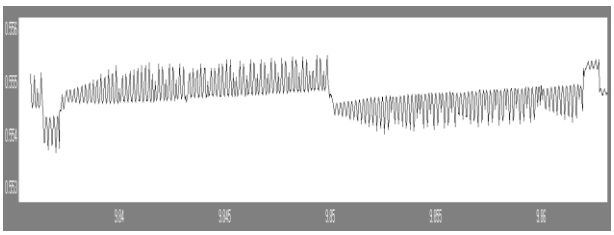

Fig-4. Output voltage

From the simulation results the output voltage is stepped down from 12V to 0.55V. when the reference voltage 2V is taken. From this tight output voltage regulation and dynamic response achieved.

Fig-5.inductor current

The output inductor current is obtained and this value is 0.715A

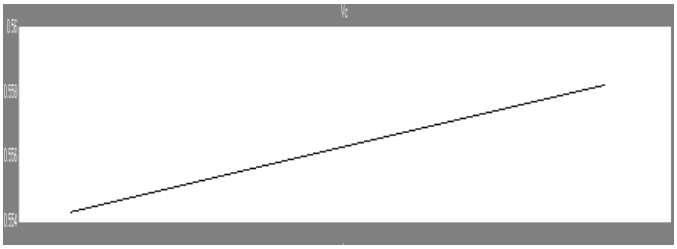

Fig-6.output capacitor voltage

The output capacitor voltage obtained with a value of 0.55V

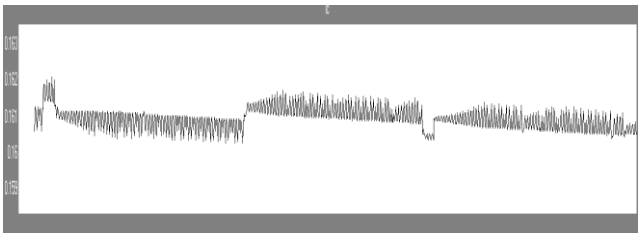

Fig-7:output capacitor current

In this proposed method ESL of the output capacitor is taken. Because of the ESL parameter the capacitor current is also taken as state variable.

V. CONCLUSION

The proposed synchronous buck converter was designed with small signal averaged model. The proposed converter should operated at the variable switching frequency by considering on time and off time of the switching period. And the multi loop PID control architecture was developed with the loop shaping of the frequency domain TF. From the simulation results tight output voltage regulation and dynamic performance is achieved.

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K.Ayyappa Received the B.Tech degree in electrical and electronics engineering from aditya engineering college surampalem ,india in 2012. And he is corrently working as a post graduate fellow in the lakireddy balireddy college of engineering, mylavaram, india. His research interests include power electronics and drives and digital controlling techniques

P.Deepak Reddy Received the B.Tech degree in electrical and electronics engineering from sreekalahasteeswara institute of technology and science, sreekalahasti, india in 2002, and he received the M.Tech degree from vellore institute of technology, vellore, india in 2005,and he is pursuing Ph.D. on "Modeling and Analysis of Control Techniques for DC-DC Buck converter" from GITAM University, Hyderabad. Currently he is working as an Assoc. Professor in Dept. of EEE in Lakireddy Balireddy college, Mylavaram india. He has published several National and International Journals.

