Distortions analysis in analog circuit with 130nm and 32nm

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Abstract - ***in analog circuit the major problem is about harmonics distortion. Sometimes this distortion comes from external environment. But almost internal harmonics distortion will change the shape of the signal. and to reduce this analysis of distortion is very important. In this paper different configuration of analog circuit using CMOS 130nm is discussed.***

Key Words: Harmonic Distortion, level 49 BSIM3 models, CMOS 32nm.

1. INTRODUCTION

In recent years, with the rise of Mixed Analog-Digital circuit design, the use of MOS transistors has not only been restricted to digital circuit design, but it has been extended to analog circuit design as well. The rise in use of MOS devices in analog circuit design is because of its high linearity feature i.e. low distortion behaviour. But, distortion is a key measure of performance for RF CMOS circuits.
Distortion is one of the most important undesired effects that appear in analog circuits. This effect will reduce if we scale down the dimensions of MOS device. But on other hand power dissipation will increase.

Types of Distortion:
1. Non-linear Distortion
2. Frequency Distortion
3. Phase-shift Distortion

1. Non-Linear Distortion-This type of distortion results from the production of new frequencies in the outputs which are not present in the input signal. These new frequencies or harmonics results from the weak non-linear behavior of circuit devices. This type of distortion is sometimes referred to as "Amplitude distortion".
When a sinusoidal input signal is applied to a circuit, the output signal will not only contain the ground harmonic but also higher-order harmonics, this is called "Harmonic distortion".

2. Frequency Distortion- This type of distortion exists when the signal of different frequencies are amplified differently. This distortion may be caused either by the internal device capacitances or it may arise because the associate circuit is reactive.

3. Phase-shift Distortion- Phase-shift distortion results from unequal phase shifts of signals of different frequencies. [1]

2. IMPLEMENTATION

All circuits have been implemented using level 49 BSIM3 models from 130nm and 32 nm CMOS process technology. The process parameters are given as follows [9]

NMOS Process Parameter	Value	PMOS Process Parameter	Value
$V_{thon}(V)$	0.37	$V_{thop}(V)$	-0.30
$T_{oxn}(m)$	2.81E-09	$T_{oxp}(m)$	2.85E-09
$\mu_{on}(m^2/V\ sec)$	0.067	$\mu_{op}(m^2/V\ sec)$	0.025
$\gamma\ (V^{1/2})$	0.46	$\gamma\ (V^{1/2})$	0.43

1. Common source amplifier with diode connected load using nmos transistors:

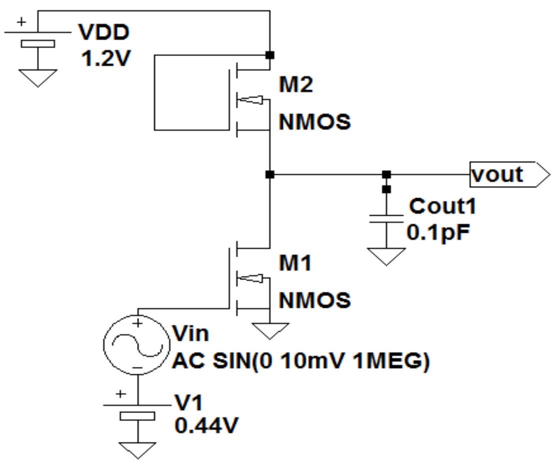

Figure 1.0: Implementing diagram of Common source amplifier with diode connected load

The design parameters are given as follows:
Supply voltage = 1.2V,
W/L ratio of driver transistor (M1) = 72,
W/L ratio of load transistor (M2) = 2,
Input bias voltage = 0.44V,
Input voltage signal level = 10mV,
Load capacitance = 0.1pF,
Operating frequency = 1MHz.

2. Cmos differential amplifier with current mirror load:

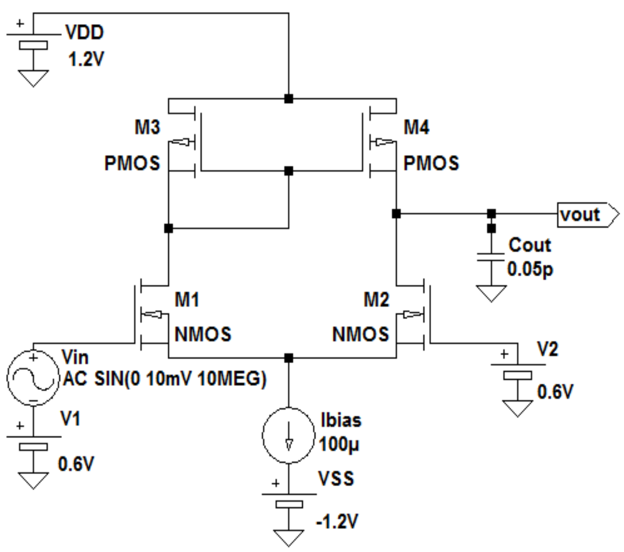

Fig1.1: Implementing diagram of CMOS differential amplifier with current mirror load.

The design parameters are given as follows:
Positive supply voltage = +1.2V,
Negative supply voltage = -1.2V
W/L ratio of driver transistors (M1 & M2) = 25,
W/L ratio of load transistors (M3 & M4) = 25,
Input bias voltage = 0.6V,
Input voltage signal level = 10mV,
Biasing current source = 100µA,
Load capacitance = 0.05pF,
Operating frequency = 10MHz.

3. Source follower with current mirror load:

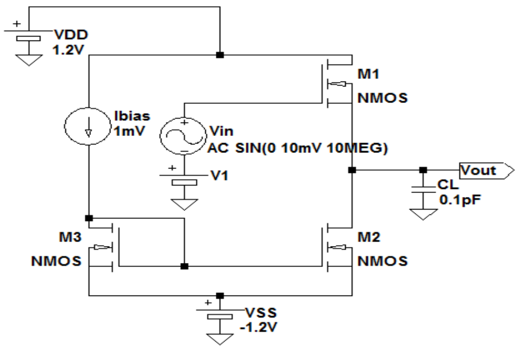

Figure 1.2: Source follower with current mirror load

The design parameters are given as follows:
Positive supply voltage = +1.2V,
Negative supply voltage = -1.2V
W/L ratio of driver transistor (M1) = 50,
W/L ratio of load transistors (M2 & M3) = 50,
Input voltage signal level = 10mV,
Biasing current source = 1mA,
Load capacitance = 0.1pF,
Operating frequency = 10MHz.

3.Result.

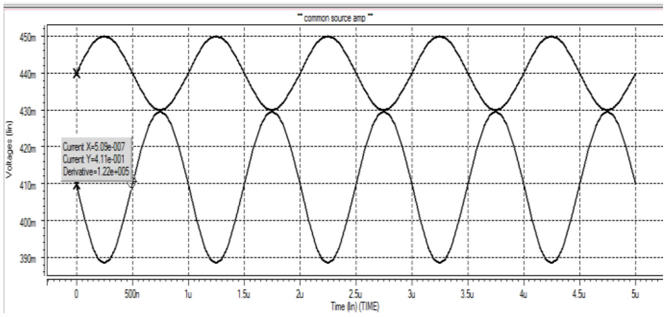

Figure 1.3.: Transient analysis of common source amplifier for 32 nm CMOS.

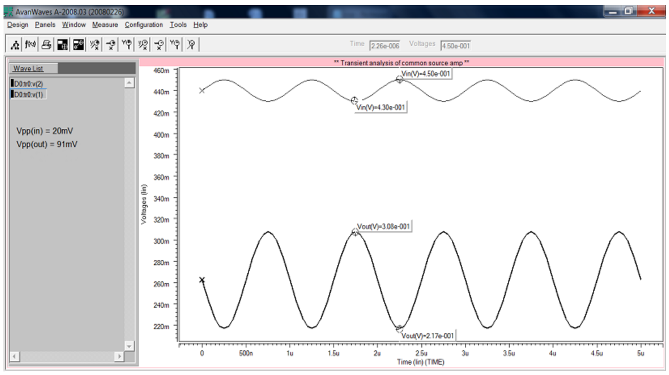

Figure 1.4.: Transient analysis of common source amplifier for 130 nm CMOS.

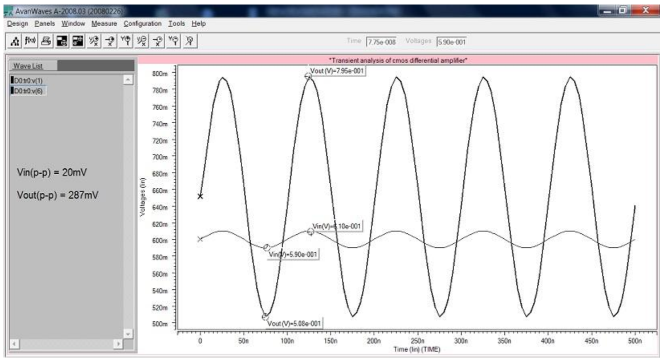

Figure 1.5.: Transient analysis of Differential amplifier for 130 nm CMOS.

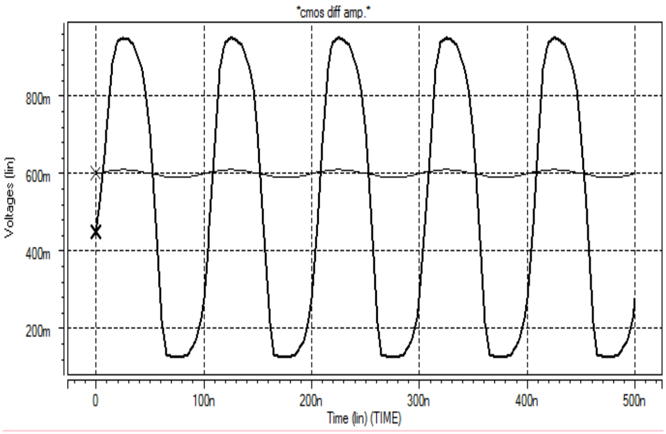

Figure 1.6.: Transient analysis of Differential amplifier for 32 nm CMOS.

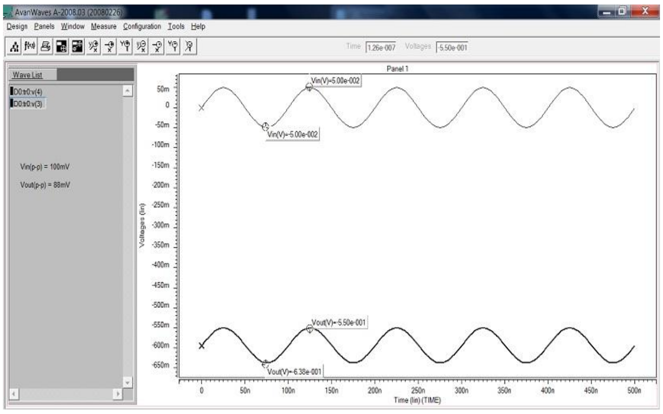

Figure 1.7: Transient analysis of source follower with current mirror amplifier for 130 nm CMOS.

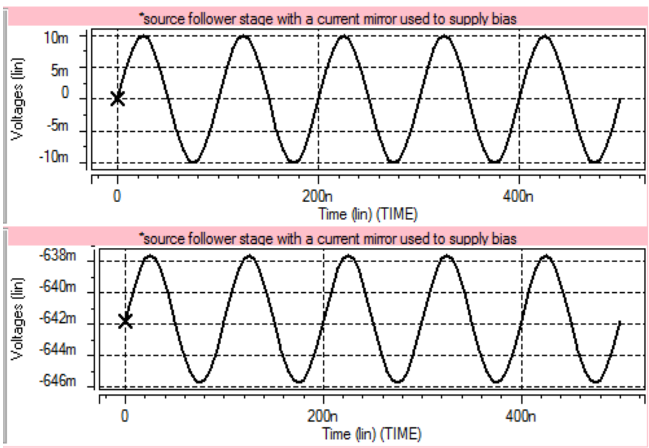

Figure 1.8.: Transient analysis of source follower amplifier for 32 nm CMOS

4. CONCLUSION.

The basic building blocks of analog integrated circuits such as Common source amplifier with diode connected load, Differential amplifier with current mirror load and Source follower with current mirror load have been chosen for distortion analysis. Distortion analysis of these cmos based circuits has been done on HSPICE tool. Different graphical plots such as Transient analysis (voltage vs. time plot), AC analysis (voltage gain vs. frequency plot), Fast Fourier Transform plot, Total Harmonic Distortion vs. Input voltage signal level and Total Harmonic Distortion vs. Frequency graph has been obtained. The presented circuit topologies have been implemented using level 49 BSIM3 models from 130nm CMOS process technology. The summary of results obtained is tabulated below:

Sr. No.	Parameters	Common Source Amplifier with diode connected load	Cmos Differential Amplifier with current mirror load	Source Follower with current mirror load
1.	Voltage gain	13.18dB	23.29dB	-1.11dB
2.	3-dB bandwidth	474 MHz	137MHz	1.62GHz
3.	Unity gain frequency (GBW)	2.10 GHz	1.89GHz	-
4.	Input voltage signal level for THD < -40dB	30mV (peak to peak)	30mV (peak to peak)	140mV (peak to peak)
5.	Frequency range for THD < -40dB	50MHz	50MHz	300MHz
6.	Power consumption	105.97µW	371.79µW	324.97mW

5.REFERENCES

1. J. Millman, Christos C. Halkias, *Integrated Electronics: Analog and Digital Circuits and Systems*, Tata McGraw-Hill, 2002.
2. C. Popa, "Linearity Evaluation Technique for CMOS Differential Amplifier", *26th International Conference on Microelectronics (MIEL 2008) NIS, Serbia* , 11-14 May, 2008.

3. Xianping Fan and P. K. Chan, "Analysis and Design of Low-Distortion CMOS Source Followers", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 52, no. 8, August 2005.
4. Melita Pennisi, Gaetano Palumbo and Ramon Gonzalez Carvajal, "Analysis and comparison of class AB current mirror OTAs", *Springer Science Business Media,* 24 October 2010.
5. Vijaya Bhadauria, Krishna Kant, Swapna Banerjee, "A Tunable Transconductor with High Linearity", *Circuits and Systems (APCCAS), 2010 IEEE Asia Pacific Conference on Kuala -Lumpur*, pp. 5 – 8, 6-9 Dec. 2010.
6. P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*, Norwel, MA Kluwer, 1998.
7. P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, Inc, 2001.
8. R. Jacob Baker, *CMOS Circuit Design Layout and Simulation*, IEEE Press and John Wiley & Sons, 3rd edition 2010.
9. B. Razavi, *Design of Analog CMOS Integrated Circuits*, Tata McGraw-Hill, 2002.
10. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Oxford Univ. Press, 2nd edition 2002.
11. Randail L. Geiger , Phillip E. Allen , Noel R. Strader, *VLSI Design Techniques for Analog and Digital Circutis*, McGRAW-Hill International Edition, 1990.
12. David Johns, Ken Martin, *Analog integrated circuit design*, John Wiley & Sons, 1997.
13. A. Sedra, K. Smith, *Microelectronic Circuits*, New York, Holt Reinhart and Winston, 1987.
14. G. Palumbo, S. Pennisi, *Feedback Amplifiers: Theory and Design*, Kluwer Academic Publishers, 2002.
15. Y. Tsividis, *Operation and Modeling of The MOS Transistor*, second edition, Oxford University Press, 1999.
16. Michael B. Steer, *SPICE:User's Guide and Reference*, Edition1.3, 2007

