Distortions analysis in analog circuit with 130nm and 32nm

Vijay jaiswal #1, G.U kharat*2.

# Department of electronics and telecommunication Sharadchandra Pawar College of Engineering, Dumberwadi, Otur pune, Maharashtra, India

Abstract - in analog circuit the major problem is about harmonics distortion. Sometimes this distortion comes from external environment. But almost internal harmonics distortion will change the shape of the signal, and to reduce this analysis of distortion is very important. In this paper different configuration of analog circuit using CMOS 130nm is discussed.

Key Words: Harmonic Distortion, level 49 BSIM3 models, CMOS 32nm.

1. INTRODUCTION

In recent years, with the rise of Mixed Analog-Digital circuit design, the use of MOS transistors has not only been restricted to digital circuit design, but it has been extended to analog circuit design as well. The rise in use of MOS devices in analog circuit design is because of its high linearity feature i.e. low distortion behaviour. But, distortion is a key measure of performance for RF CMOS circuits. Distortion is one of the most important undesired effects that appear in analog circuits. This effect will reduce if we scale down the dimensions of MOS device. But on other hand power dissipation will increase.

Types of Distortion:
1. Non-linear Distortion
2. Frequency Distortion
3. Phase-shift Distortion

1. Non-Linear Distortion-This type of distortion results from the production of new frequencies in the outputs which are not present in the input signal. These new frequencies or harmonics results from the weak non-linear behavior of circuit devices. This type of distortion is sometimes referred to as “Amplitude distortion”.

When a sinusoidal input signal is applied to a circuit, the output signal will not only contain the ground harmonic but also higher-order harmonics, this is called “Harmonic distortion”.

2. Frequency Distortion- This type of distortion exists when the signal of different frequencies are amplified differently. This distortion may be caused either by the internal device capacitances or it may arise because the associate circuit is reactive.

3. Phase-shift Distortion- Phase-shift distortion results from unequal phase shifts of signals of different frequencies. [1]

2. IMPLEMENTATION

All circuits have been implemented using level 49 BSIM3 models from 130nm and 32 nm CMOS process technology. The process parameters are given as follows [9]

<table>
<thead>
<tr>
<th>NMOS Process Parameter</th>
<th>Value</th>
<th>PMOS Process Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{th} (V)$</td>
<td>0.37</td>
<td>$V_{th} (V)$</td>
<td>-0.30</td>
</tr>
<tr>
<td>$T_{o,xn} (m)$</td>
<td>2.81E-09</td>
<td>$T_{o,xp} (m)$</td>
<td>2.85E-09</td>
</tr>
<tr>
<td>$\mu_{ox} (m^2/V sec)$</td>
<td>0.067</td>
<td>$\mu_{op} (m^2/V sec)$</td>
<td>0.025</td>
</tr>
<tr>
<td>$\gamma (V^{1/2})$</td>
<td>0.46</td>
<td>$\gamma (V^{1/2})$</td>
<td>0.43</td>
</tr>
</tbody>
</table>

1. Common source amplifier with diode connected load using nmos transistors:

![Figure 1.0: Implementing diagram of Common source amplifier with diode connected load](image-url)
The design parameters are given as follows:
Supply voltage = 1.2V,
W/L ratio of driver transistor (M1) = 72,
W/L ratio of load transistor (M2) = 2,
Input bias voltage = 0.44V,
Input voltage signal level = 10mV,
Load capacitance = 0.1pF,
Operating frequency = 1MHz.

2. CMOS differential amplifier with current mirror load:

![Diagram of CMOS differential amplifier with current mirror load]

The design parameters are given as follows:
Positive supply voltage = +1.2V,
Negative supply voltage = -1.2V
W/L ratio of driver transistors (M1 & M2) = 25,
W/L ratio of load transistors (M3 & M4) = 25,
Input bias voltage = 0.6V,
Input voltage signal level = 10mV,
Biasing current source = 100µA,
Load capacitance = 0.05pF,
Operating frequency = 10MHz.

3. Source follower with current mirror load:

![Diagram of source follower with current mirror load]

The design parameters are given as follows:
Positive supply voltage = +1.2V,
Negative supply voltage = -1.2V
W/L ratio of driver transistor (M1) = 50,
W/L ratio of load transistors (M2 & M3) = 50,
Input voltage signal level = 10mV,
Biasing current source = 1mA,
Load capacitance = 0.1pF,
Operating frequency = 10MHz.

3. Result.

![Figure 1.3: Transient analysis of common source amplifier for 32 nm CMOS]

![Figure 1.4: Transient analysis of common source amplifier for 130 nm CMOS]

![Figure 1.5: Transient analysis of Differential amplifier for 130 nm CMOS]
4. CONCLUSION.

The basic building blocks of analog integrated circuits such as Common source amplifier with diode connected load, Differential amplifier with current mirror load and Source follower with current mirror load have been chosen for distortion analysis. Distortion analysis of these cmos based circuits has been done on HSPICE tool. Different graphical plots such as Transient analysis (voltage vs. time plot), AC analysis (voltage gain vs. frequency plot), Fast Fourier Transform plot, Total Harmonic Distortion vs. Input voltage signal level and Total Harmonic Distortion vs. Frequency graph has been obtained. The presented circuit topologies have been implemented using level 49 BSIM3 models from 130nm CMOS process technology. The summary of results obtained is tabulated below:

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Parameters</th>
<th>Common Source Amplifier with diode connected load</th>
<th>Cmos Differential Amplifier with current mirror load</th>
<th>Source Follower with current mirror load</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Voltage gain</td>
<td>13.18dB</td>
<td>23.29dB</td>
<td>-1.11dB</td>
</tr>
<tr>
<td>2.</td>
<td>3-dB bandwidth</td>
<td>474 MHz</td>
<td>137MHz</td>
<td>1.62GHz</td>
</tr>
<tr>
<td>3.</td>
<td>Unity gain frequency (GBW)</td>
<td>2.10 GHz</td>
<td>1.89GHz</td>
<td>-</td>
</tr>
<tr>
<td>4.</td>
<td>Input voltage signal level for THD &lt; -40dB</td>
<td>30mV (peak to peak)</td>
<td>30mV (peak to peak)</td>
<td>140mV (peak to peak)</td>
</tr>
<tr>
<td>5.</td>
<td>Frequency range for THD &lt; -40dB</td>
<td>50MHz</td>
<td>50MHz</td>
<td>300MHz</td>
</tr>
<tr>
<td>6.</td>
<td>Power consumption</td>
<td>105.97µW</td>
<td>371.79µW</td>
<td>324.97mW</td>
</tr>
</tbody>
</table>

5. REFERENCES


