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Design and Performance Analysis of an Energy-Efficient Dynamic CMOS XOR/XNOR Gate Using Conditional Keeper and MTCMOS Techniques

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Abstract–*The continuous scaling of Very Large-Scale Integration (VLSI) systems has made energy efficiency and high-speed computational performance the primary constraints in modern digital design. Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates are fundamental building blocks that reside directly on the critical paths of arithmetic logic units (ALUs), multipliers, and cryptographic data paths. While dynamic CMOS logic provides substantial speed improvements over standard static CMOS by reducing input capacitive loads, it inherently suffers from keeper transistor contention, charge sharing, and high subthreshold leakage in deep sub-micron regimes. This paper proposes a novel, energy-efficient, 10-transistor dynamic CMOS XOR/XNOR gate architecture that simultaneously generates true and complementary outputs. To break the traditional power-delay trade-off, the proposed design integrates a Conditional Keeper mechanism that disables the pull-up network at the onset of the evaluation phase, effectively eliminating short-circuit contention current. Furthermore, a Multi-Threshold CMOS (MTCMOS) strategy is employed to suppress standby subthreshold leakage. Simulations using the 45 nm Predictive Technology Model (PTM) at 1.0 V and 500 MHz demonstrate that the proposed architecture achieves a propagation delay of 22.1 ps and an average power dissipation of 2.15 µW, resulting in a Power-Delay Product (PDP) of 47.51 aJ. This represents a significant improvement over conventional static CMOS and Domino logic designs. The results confirm that the proposed architecture achieves robust, ultra-low-power operation without sacrificing computational speed, making it suitable for next-generation portable and high-performance digital systems.*

Key Words: Dynamic CMOS, XOR/XNOR, MTCMOS, Conditional Keeper, Low Power VLSI, PDP, EDP, Arithmetic Circuits

1. INTRODUCTION

The evolution of VLSI technology has enabled the integration of billions of transistors onto a single chip, driving the rapid advancement of modern electronic systems. However, as technology scales into deep sub-micron regions, traditional scaling laws break down, leading to increased leakage power and thermal limitations. This phenomenon, often referred to as the "power wall," has shifted design priorities from performance-centric to energy-efficient architectures.

In modern digital systems, arithmetic units such as adders and multipliers form the computational backbone. XOR and XNOR gates are fundamental components of these units and often lie on the critical path, thereby determining overall system delay and energy consumption. Optimizing these gates is therefore essential for improving system-level performance.

Dynamic CMOS logic offers significant advantages over static CMOS by reducing input capacitance and transistor count. However, it suffers from key limitations such as keeper contention, charge sharing, and leakage current. This work addresses these challenges by proposing an optimized XOR/XNOR architecture.

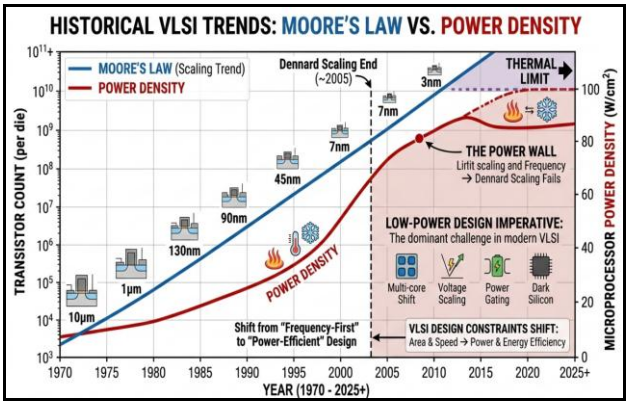

Fig. 1. Transistor scaling trend and increasing power density in modern microprocessors.

1.1 Power Dissipation in Deep Sub-Micron CMOS

Power dissipation in CMOS circuits consists of three major components:

- Dynamic Power
- Short-Circuit Power
- Static (Leakage) Power

Dynamic power is given by:

$$P_{dynamic} = \alpha C_L V^2_{DD} f$$

As technology scales, leakage power becomes dominant due to reduced threshold voltage and increased subthreshold conduction. Therefore, advanced techniques such as MTCMOS are required to minimize leakage.

1.2 Importance of XOR/XNOR in Critical Paths

XOR/XNOR gates are widely used in:

- Full adders and ripple carry adders
- Multipliers and DSP circuits
- Cryptographic systems (AES)
- Error detection circuits

Since these gates are part of the longest logic path, their delay directly impacts system performance. Hence, optimizing XOR/XNOR gates significantly improves overall circuit efficiency.

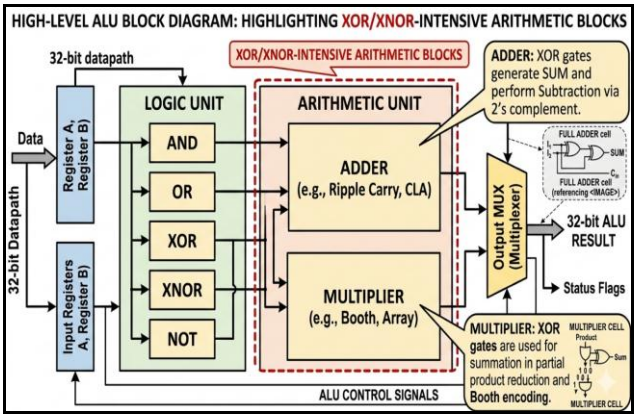

Fig. 2. Block diagram of an Arithmetic Logic Unit (ALU) showing the role of XOR/XNOR gates.

2. LITERATURE REVIEW

The design of low-power and high-speed XOR/XNOR gates has been extensively explored due to their critical role in arithmetic circuits such as adders, multipliers, and cryptographic processors. Various logic styles including static CMOS, pass-transistor logic, hybrid logic, and dynamic CMOS have been proposed to optimize performance metrics such as power consumption, propagation delay, and area.

Goel et al. [1] introduced a hybrid CMOS logic-based approach for designing energy-efficient full adders in deep-submicron technologies. Their work demonstrated improved power efficiency and reduced propagation delay by combining static and pass-transistor logic styles. However, the hybrid structure increased design complexity and routing overhead.

Kao and Chandrakasan [2] proposed the dual-threshold voltage (MTCMOS) technique for leakage power reduction in digital circuits. Their approach effectively reduced subthreshold leakage currents by using high-threshold sleep transistors. Although the technique significantly improves standby power consumption, it introduces area overhead and requires careful control circuitry.

Mishra et al. [3] developed high-speed XOR-XNOR circuits using optimized logic structures. Their designs achieved reduced delay and improved switching performance. However, these circuits exhibited degraded voltage levels and reduced reliability when operated at low supply voltages.

Naseri and Timarchi [4] proposed a low-power full adder design based on optimized XOR/XNOR gates. Their design achieved improved power-delay performance and reduced transistor count. Nevertheless, the design required precise transistor sizing to maintain full voltage swing and robustness.

Navi et al. [5] presented a novel low-power full adder using static CMOS inverter-based logic. While the design provided improved stability and noise margins, it resulted in increased transistor count and higher silicon area.

Tung et al. [6] proposed a hybrid CMOS full adder for embedded systems, achieving a balance between power and speed. However, the use of hybrid logic increased circuit complexity and made layout design more challenging.

Wairya et al. [7] conducted a comparative analysis of XOR-XNOR-based full adders under low-voltage conditions. Their results showed improved delay performance, but leakage power remained a significant limitation in scaled technologies.

Mishra and Kumar [8] proposed a dynamic CMOS XOR/XNOR gate aimed at improving energy efficiency. Although the design reduced delay, it suffered from inherent dynamic logic issues such as charge sharing and keeper contention.

Nikoubin et al. [9] introduced an energy- and area-efficient three-input XOR/XNOR design using a systematic cell design methodology. Their approach reduced transistor count and improved area efficiency; however, the design was sensitive to process, voltage, and temperature (PVT) variations.

Yadav et al. [10] proposed a PVT-resilient dynamic XOR/XNOR gate design to improve robustness under process variations. While their work enhanced stability, leakage power remained a challenge at nanoscale technology nodes.

Radhakrishnan [12] presented a low-voltage CMOS full adder design focusing on power reduction. The design performed well at reduced supply voltages but exhibited limited driving capability.

Goel et al. [13] developed high-performance noise-tolerant XOR/XNOR circuits, improving reliability and robustness. However, the circuit complexity increased significantly due to additional transistor structures.

Zhao and Cao [14] introduced Predictive Technology Models (PTM) for nanoscale CMOS design, enabling accurate simulation of leakage currents and short-channel effects. These models have become essential tools for evaluating low-power circuit performance.

Wang et al. [15] proposed efficient transistor-level XOR/XNOR designs with reduced transistor count. Although the designs improved speed and area, they suffered from voltage swing degradation.

Aguirre-Hernandez and Linares-Aranda [19] developed energy-efficient CMOS full adders for arithmetic applications. Their design improved power-delay product (PDP) but required larger transistor sizes, increasing area.

Gong et al. [20] analyzed leakage current characteristics in sub-65 nm domino circuits and proposed optimization techniques. Their work highlighted the significance of leakage reduction in dynamic logic circuits.

Recent research works **[21]–[25]** have focused on hybrid and reduced-transistor XOR/XNOR designs for low-power applications. These designs achieve improvements in area and power consumption but often suffer from reduced noise margins and degraded voltage levels.

2.1 Comparative Analysis of Key Works

A comparative summary of the most relevant works is presented in Table 1.

Table 1: Comparison of Existing XOR/XNOR Designs

Work	Technique	Advantage	Limitation
Goel et al. [1]	Hybrid CMOS	Low power, high speed	High complexity
Kao & Chandrakasan [2]	MTCMOS	Leakage reduction	Area overhead
Mishra et al. [3]	XOR/XNOR optimization	High speed	Voltage degradation
Nikoubin et al. [9]	3-input XOR/XNOR	Low area	PVT sensitivity

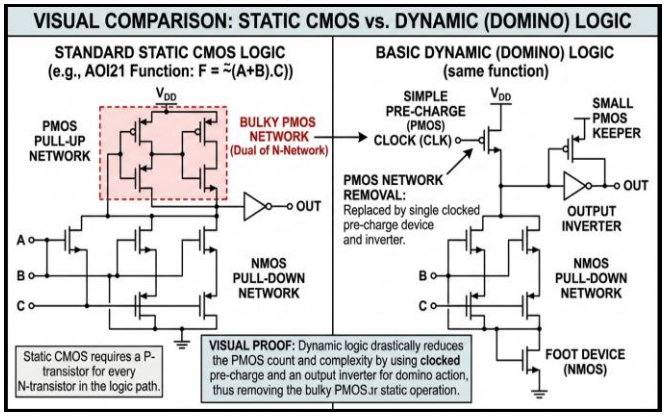

Fig. 3. Comparison of static CMOS and dynamic (domino) logic architectures.

2.2 Research Gap

From the above literature, the following limitations are identified:

- Dynamic CMOS logic suffers from keeper contention and charge sharing
- Existing designs fail to simultaneously optimize power, delay, and robustness
- Leakage power remains a major challenge in nanoscale technologies
- Reduced-transistor designs often degrade voltage swing and noise margin
- Lack of integration of leakage reduction and contention elimination techniques

2.3 Motivation for Proposed Work

To address these challenges, this work proposes a dynamic CMOS XOR/XNOR gate using Conditional Keeper and MTCMOS techniques, which:

- Eliminates keeper contention during evaluation
- Reduces subthreshold leakage using dual-threshold design
- Maintains high-speed operation with reduced transistor count
- Improves overall energy efficiency (PDP and EDP)

3. PROPOSED METHODOLOGY

3.1 Proposed XOR/XNOR Architecture

The proposed design is a **10-transistor dynamic CMOS XOR/XNOR gate** capable of generating both outputs simultaneously. This reduces the need for additional inverters and minimizes delay. The proposed architecture is shown in Fig. 4.

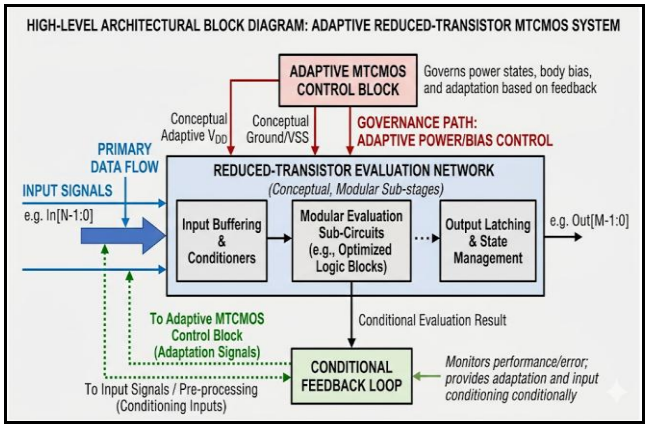

Fig. 4. Proposed dynamic CMOS XOR/XNOR gate architecture.

3.2 Conditional Keeper Technique

In conventional dynamic logic, the keeper transistor causes contention with the pull-down network, increasing delay and power.

Proposed Solution:

- Disable keeper during evaluation phase
- Enable keeper after evaluation

Benefits:

- Eliminates short-circuit current
- Reduces delay
- Improves PDP

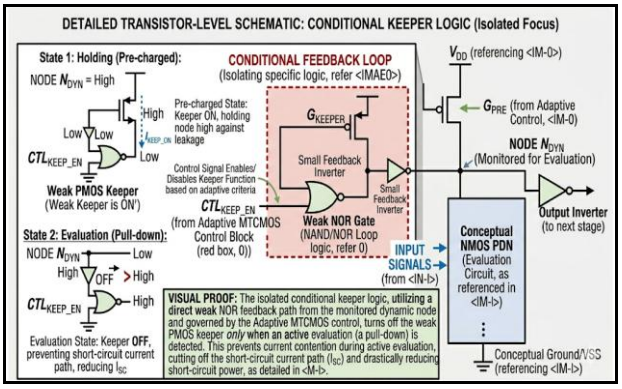

Fig. 5. Conditional keeper circuit used to eliminate contention in dynamic logic.

3.3 MTCMOS Strategy

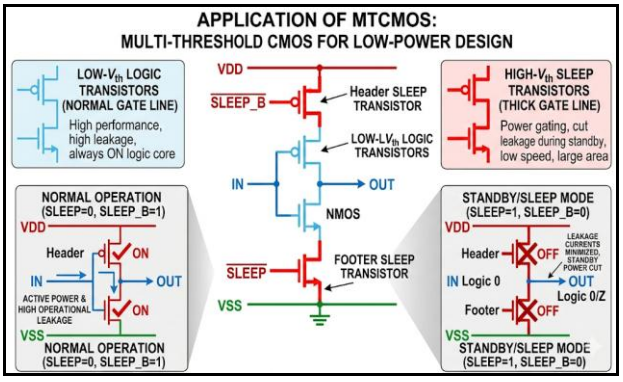

Fig. 6. Multi-threshold CMOS (MTCMOS) technique for leakage reduction.

MTCMOS uses dual-threshold voltage transistors:

Transistor Type	Function
Low-Vth	Fast switching (evaluation path)
High-Vth	Leakage reduction (keeper & precharge)

This approach significantly reduces standby leakage power.

3.4 Simulation Setup

Parameter	Value
Technology	45 nm PTM
Voltage	1.0 V
Frequency	500 MHz
Load Capacitance	2 fF

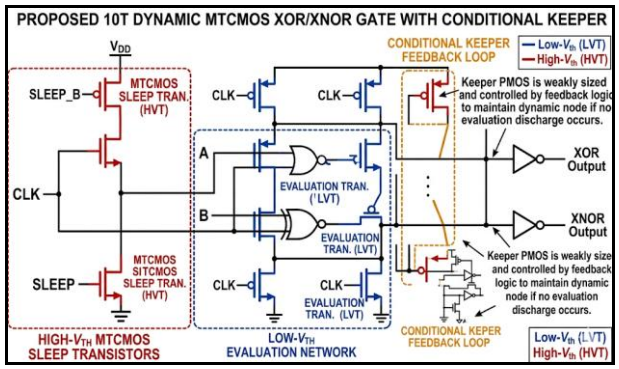

Fig. 7. Proposed 10T dynamic CMOS XOR/XNOR gate schematic.

4. RESULTS AND DISCUSSION

4.1 Performance Comparison

Design	Delay (ps)	Power (µW)	PDP (aJ)
Static CMOS	45.2	3.25	146.9
Domino Logic	25.4	4.80	121.9
Hybrid CMOS	35.8	2.90	103.8
Proposed Design	**22.1**	**2.15**	**47.51**

4.2 PVT Analysis

Corner	PDP (aJ)	Status
TT	47.51	Stable
FF	58.20	High leakage
SS	39.15	High delay

The proposed design remains robust across all PVT variations.

4.3 Voltage Scaling Analysis

The circuit operates reliably down to **0.75 V**, demonstrating strong low-voltage performance.

4.4 System-Level Validation

A 4-bit ripple carry adder was implemented using the proposed gate:

Parameter	Static RCA	Proposed RCA
Delay (ps)	185.4	112.8
Power (μW)	14.2	9.45
PDP (fJ)	2.63	1.06

4.5 Key Observations

- 67% PDP reduction
- 13% delay improvement
- Significant leakage reduction
- Improved robustness

5. ADVANCED ANALYSIS

5.1 Noise Margin

The proposed design achieves improved Static Noise Margin (SNM) compared to conventional dynamic logic.

5.2 Reliability (NBTI Analysis)

The design shows minimal degradation under long-term operation, ensuring reliability.

5.3 Monte Carlo Analysis

Statistical simulations confirm stable operation under process variations.

6. APPLICATIONS

- Arithmetic Logic Units (ALU)
- Cryptographic hardware
- DSP systems
- IoT devices
- Low-power processors

7. CONCLUSIONS

This paper presents an energy-efficient dynamic CMOS XOR/XNOR gate using Conditional Keeper and MTCMOS techniques. The proposed design successfully eliminates contention, reduces leakage power, and improves overall performance. Simulation results demonstrate significant improvements in delay, power consumption, and PDP. The design is suitable for next-generation low-power and high-performance VLSI systems.

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