

Introduction to Instruction Pipelining in CPU Architecture: A Review

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Abstract - Instruction pipelining is a fundamental performance enhancement technique in modern CPU architectures that enables the overlapping of instruction execution stages, thereby improving throughput and resource utilization. Over the past few decades, pipelining has evolved from simple five-stage RISC designs to sophisticated multi-issue, superscalar, and out-of-order execution models integrated in today's high-performance processors. This review presents a comprehensive analysis of instruction pipelining concepts, focusing on pipeline stages, types of hazards, hazard detection and mitigation strategies, and design trade-offs. It synthesizes findings from fifteen recent and classical research papers addressing topics such as hazard prediction mechanisms, stall reduction, dynamic scheduling, low-power pipeline optimization, and simulation-based learning approaches. The paper highlights comparative insights from different pipeline architectures, including MIPS, RISC-V, and ARM designs, and discusses how pipeline depth, forwarding logic, and speculative execution influence performance and energy efficiency. Furthermore, it identifies emerging research trends in adaptive and AI-assisted pipelining, as well as the continuing challenges in balancing power, complexity, and speed. This review aims to provide a foundational understanding for students and researchers exploring the design and optimization of pipelined CPU architectures.

Key Words: Instruction Pipelining, CPU Architecture, Pipeline Hazards, Data Hazard, Control Hazard, Structural Hazard, RISC Architecture, MIPS Processor, Superscalar Design, Out-of-Order Execution, Pipeline Optimization, Hazard Detection, Dynamic Scheduling, Low-Power Pipeline, Performance Enhancement.

1. INTRODUCTION

In modern computer systems, performance is often determined by how efficiently a processor can execute instructions. As software applications have grown increasingly complex, the need for faster and more efficient hardware execution has become critical. One of the most effective techniques introduced to enhance CPU performance is instruction pipelining. This concept allows multiple instructions to be processed simultaneously by

dividing their execution into several distinct stages, with each stage performing a specific part of the instruction cycle.

Instruction pipelining works on the principle of overlapping instruction execution—while one instruction is being decoded, another can be fetched, and a third can be executed. This overlapping significantly improves processor throughput, as multiple instructions are in different stages of execution at any given time. Essentially, pipelining transforms the processor into an assembly line, where different components work concurrently to complete tasks faster and more efficiently.

The introduction of pipelining marked a major advancement in CPU architecture. It laid the foundation for many subsequent innovations such as superscalar processing, out-of-order execution, and speculative branching. These advancements aim to exploit instruction-level parallelism (ILP), allowing processors to perform more work per clock cycle without increasing the clock frequency. As a result, pipelining has become a central feature of most modern processors, ranging from embedded systems to high-performance computing platforms.

However, the efficiency of a pipelined processor is not absolute. Real-world performance can be affected by several challenges known as pipeline hazards, which include data, control, and structural hazards. These hazards occur when instructions depend on the results of previous ones, when branching disrupts the instruction flow, or when hardware resources are shared among multiple instructions. To mitigate these challenges, various techniques such as forwarding, stalling, and branch prediction are used to maintain smooth execution and prevent performance degradation.

In addition to improving speed, modern pipeline designs also focus on reducing power consumption and optimizing transistor usage. Deep pipelines and parallel pipelines have been developed to strike a balance between performance, power, and cost. With the continuous evolution of computing technology, pipelining remains a

critical area of research, influencing both the theoretical and practical aspects of computer architecture.

This review aims to provide a comprehensive understanding of instruction pipelining in CPU architecture, covering its basic principles, operational stages, challenges, optimization techniques, and modern implementations. It also discusses how pipelining continues to evolve to meet the demands of contemporary computing systems and future processor designs.

2.BACKGROUND AND FUNDAMENTALS OF INSTRUCTION PIPELINING

Instruction pipelining is a technique used in CPU architecture to improve the instruction throughput by overlapping the execution of multiple instructions. Instead of executing one instruction completely before fetching the next, pipelining divides the instruction execution process into several smaller stages, where each stage performs a specific operation on different instructions concurrently. This approach allows a new instruction to enter the pipeline every clock cycle, effectively increasing overall system performance.

2.1 Basic Concept

The idea of instruction pipelining is analogous to an assembly line in industrial manufacturing. Each instruction goes through a series of well-defined stages, and while one stage is processing one instruction, the other stages process other instructions in parallel. Theoretically, if there are n stages in a pipeline, the maximum speedup over a non-pipelined processor can approach n times, assuming ideal conditions and no stalls. This relationship can be expressed as:

$$\text{Speedup} = \frac{\text{Time}_{\text{unpipelined}}}{\text{Time}_{\text{pipelined}}} \approx n$$

However, real-world performance is often less than ideal due to hazards, resource conflicts, and branch mispredictions.

2.2 Pipeline Stages

A typical RISC pipeline, as used in MIPS or ARM processors, consists of five fundamental stages [1]-[3]:

1. **Instruction Fetch (IF):** The CPU fetches the next instruction from memory and increments the program counter.
2. **Instruction Decode (ID):** The fetched instruction is decoded, and the required registers are identified and read.
3. **Execution (EX):** Arithmetic or logical operations are performed using the Arithmetic Logic Unit (ALU).

4. **Memory Access (MEM):** Memory is accessed for load or store operations.
5. **Write Back (WB):** The result is written back to the destination register.

Each stage is synchronized using a common system clock, and intermediate results are stored in pipeline registers. These registers isolate one stage from another, allowing simultaneous execution of multiple instructions.

2.3 Pipeline Operation Flow

In a pipelined processor, instructions progress through the pipeline in sequential order, but several instructions are in different stages of execution at the same time. For example, while one instruction is in the *Execute* stage, another may be in the *Decode* stage, and yet another in the *Fetch* stage. This concurrent execution greatly enhances throughput, as one instruction completes on every clock cycle after the pipeline is filled.

Table I demonstrates a simplified timeline for a five-stage pipeline executing four consecutive instructions (I_1 to I_4). Each column represents a clock cycle.

Cycle	I1	I2	I3	I4	...
1	IF				
2	ID	IF			
3	EX	ID	IF		
4	MEM	EX	ID	IF	
5	WB	MEM	EX	ID	
6		WB	MEM	EX	
7			WB	MEM	
8				WB	

Table -1: pipeline execution flow for a five-stage pipeline

This demonstrates that once the pipeline is full, one instruction completes at every cycle, providing higher throughput compared to non-pipelined architectures.

2.4 Ideal vs. Non-Ideal Pipeline Performance

Under ideal conditions, a five-stage pipeline can yield a speedup close to five times that of a sequential processor. However, in practical implementations, issues such as *pipeline stalls*, *data dependencies*, and *branch mispredictions* introduce bubbles into the pipeline, reducing efficiency [4], [5]. Techniques such as *data forwarding*, *branch prediction*, and *speculative execution* have been developed to minimize these effects.

Furthermore, deep pipelines, while increasing the clock frequency, can also increase branch penalties and power consumption. Designers must therefore find a trade-off between pipeline depth, complexity, and energy efficiency [5], [6]. Studies in [7], [8] have shown that intelligent

pipeline balancing and hazard detection circuits can maintain performance while minimizing power overhead.

2.5 Summary

The fundamentals of instruction pipelining establish the foundation for understanding subsequent challenges and optimizations. While the five-stage pipeline serves as the baseline model for educational and RISC-based designs, modern processors often use deeper and wider pipelines with advanced scheduling and prediction mechanisms. The next section discusses the primary types of pipeline hazards and various methods proposed in literature to handle them efficiently.

3. PIPELINE HAZARDS AND HANDLING TECHNIQUES

Although instruction pipelining improves CPU performance by overlapping instruction execution, it introduces a set of challenges known as *pipeline hazards*. These hazards prevent the next instruction in the pipeline from executing during its designated clock cycle, thereby reducing the overall efficiency of the processor. Hazards are generally categorized into three types: *data hazards*, *control hazards* and *structural hazards*. Understanding and resolving these issues is fundamental to achieving optimal pipeline performance [1], [4] [9].

3.1 Data Hazards

Data hazards occur when an instruction depends on the result of a previous instruction that has not yet completed its execution. They are further divided into three subtypes:

- **Read After Write (RAW)** – Occurs when an instruction needs to read a register before the previous instruction writes its result to that register.
- **Write After Read (WAR)** – Occurs when an instruction writes to a register before a previous instruction has read from it.
- **Write After Write (WAW)** – Occurs when two instructions write to the same register in the wrong order.

To mitigate data hazards, several techniques have been proposed. The most common methods include:

- **Data Forwarding (Bypassing):** Introduces additional hardware paths that forward intermediate results directly to dependent instructions without waiting for them to be written back to the register file [3], [5].
- **Pipeline Interlocking:** The processor automatically detects data dependencies and introduces *stalls* (bubbles) into the pipeline until the required data is available.

- **Compiler Scheduling:** Compilers can reorder instructions at compile-time to avoid pipeline stalls, known as *instruction scheduling*.

Recent studies, such as Chen and Park's hazard detection method [4], employ combinational logic and hazard detection units to automatically identify RAW dependencies and dynamically insert stalls when necessary. Similarly, Hossain and Rahman [10] proposed a pipeline control unit for five-stage RISC architectures that improves hazard resolution efficiency while maintaining throughput.

3.2 Control Hazards

Control hazards, also known as *branch hazards*, occur when the pipeline makes wrong assumptions about the flow of control—typically due to conditional branch instructions. Since the next instruction depends on whether a branch is taken or not, the pipeline must stall until the branch outcome is known, resulting in performance penalties.

Modern processors employ several branch prediction and speculative execution techniques to mitigate control hazards:

- **Static Branch Prediction:** Uses predefined rules such as “assume branch not taken” to decide the next instruction.
- **Dynamic Branch Prediction:** Utilizes hardware mechanisms that record historical branch behavior to predict future outcomes more accurately [11], [12].
- **Delayed Branching:** Reorders instructions so that useful operations execute in the branch delay slot.
- **Speculative Execution:** Executes both paths of a branch and discards incorrect results once the branch direction is resolved.

Kim and Lee [5] demonstrated that accurate branch prediction combined with power-aware speculation can significantly reduce energy consumption and stall frequency. Similarly, adaptive reconfigurable pipelines [13] dynamically adjust their depth based on branch prediction accuracy, minimizing wasted cycles and improving performance.

3.3 Structural Hazards

Structural hazards occur when two or more instructions require the same hardware resource simultaneously, such as memory ports, ALUs, or register files. These hazards are typically caused by insufficient hardware resources or poor design partitioning [1], [9].

Common solutions to structural hazards include:

- **Resource Duplication:** Adding multiple hardware units (e.g., additional ALUs or memory ports) to eliminate contention.
- **Pipeline Balancing:** Designing pipeline stages to have equal execution time to prevent resource bottlenecks [6].
- **Time-Multiplexing:** Scheduling the use of a shared resource at different cycles to avoid conflicts.

Wang and Li [6] proposed a power-efficient pipelined architecture for embedded processors that uses resource-aware balancing techniques to mitigate structural hazards while minimizing energy overhead.

3.4 Combined Hazard Handling and Modern Techniques

In modern superscalar and multicore CPUs, hazards are often interdependent, requiring integrated solutions. Advanced architectures incorporate *scoreboarding*, *Tomasulo's algorithm*, and *out-of-order execution* to manage multiple hazards concurrently. These methods allow the CPU to track instruction dependencies dynamically and issue instructions out of sequence while maintaining program correctness [2], [12].

Furthermore, simulation-based studies such as Patel and Kumar's educational model [14] demonstrate how interactive simulators can visualize hazards, stalls, and forwarding paths, aiding students in understanding complex pipeline behaviors. Emerging research trends also explore AI-assisted hazard prediction, which uses neural networks to forecast pipeline stalls before they occur, improving performance and reducing power usage.

3.5 Summary

Pipeline hazards represent a fundamental limitation in achieving ideal pipeline performance. However, continuous advancements in hazard detection, prediction, and mitigation strategies—ranging from hardware-based interlocks to machine learning models—have significantly improved efficiency. The next section reviews optimization techniques and architectural enhancements that further refine pipeline operation and throughput.

4. OPTIMIZATION TECHNIQUES AND MODERN IMPLEMENTATIONS

Instruction pipelining has evolved considerably over the years, with continuous innovations aimed at improving throughput, energy efficiency, and hardware utilization. While early designs focused on fixed five-stage pipelines, modern architectures integrate multiple optimization techniques to handle increasing instruction complexity and parallelism. This section reviews the most prominent

optimization techniques and implementation strategies in recent CPU designs.

4.1 Superscalar and Out-of-Order Execution

Superscalar architectures issue and execute multiple instructions per clock cycle by employing multiple functional units. Out-of-order (OOO) execution further enhances performance by allowing instructions to be executed as soon as their operands are available, irrespective of program order. These features significantly mitigate pipeline stalls caused by data dependencies and control hazards [2],[9],[12].

Tomasulo's algorithm remains one of the most widely adopted approaches for dynamic scheduling in OOO architectures. It uses register renaming and reservation stations to eliminate WAR and WAW hazards while efficiently managing data forwarding. Recent designs combine Tomasulo's algorithm with speculative execution to achieve high instruction throughput, as demonstrated in adaptive OOO processors [11].

4.2 Pipeline Depth Optimization

The performance of a pipeline is closely tied to its depth—the number of stages through which an instruction passes. While deeper pipelines increase instruction throughput, they also heighten the risk of hazards and increase branch misprediction penalties. Designers must therefore balance performance gains against complexity and power consumption [5].

Studies by Kim and Lee [5] reveal that optimizing pipeline depth with respect to workload characteristics can yield significant energy savings. Adaptive-depth pipelines that dynamically adjust the number of active stages based on runtime behavior have also been proposed [13] allowing processors to maintain high performance under varying load conditions.

4.3 Low-Power Pipeline Design

With the proliferation of embedded and mobile systems, reducing power consumption has become a central design goal. Low-power pipelining techniques focus on minimizing unnecessary transitions, idle cycles, and redundant computations. Strategies include:

- **Clock Gating:** Disabling the clock for inactive pipeline stages to save dynamic power.
- **Operand Gating:** Preventing unnecessary switching activity in combinational logic.
- **Pipeline Throttling:** Dynamically adjusting the clock frequency based on workload.

A power-aware pipeline model proposed by Kim et al. [5] integrates adaptive clock gating and speculative execution

control to minimize energy waste without compromising throughput. Similarly, Wang and Li [6] introduced a resource-aware design for embedded processors that achieves over 20% energy savings while maintaining instruction throughput.

4.4 RISC-V and Modular Pipeline Architectures

The RISC-V architecture has emerged as an open-source alternative to traditional proprietary designs like ARM and x86. Its modular instruction set architecture (ISA) allows designers to customize pipeline stages based on performance and application needs. The standard five-stage RISC-V pipeline—comprising *Fetch*, *Decode*, *Execute*, *Memory*, and *Writeback*—serves as a foundation for both academic and industrial designs [2],[10].

Recent implementations integrate additional stages such as instruction buffering and branch prediction, leading to enhanced parallelism and performance. Hossain and Rahman [10] designed a modified five-stage RISC pipeline incorporating dynamic hazard detection and forwarding logic, achieving higher instruction throughput compared to conventional MIPS-based systems. Similarly, the RISC-V RV32I pipeline simulation presented by Patel and Kumar [14] demonstrates educational advantages in visualizing instruction flow and hazard handling.

4.5 Speculative and Predictive Optimization Techniques

Speculative execution and predictive models play vital roles in maintaining instruction throughput despite control dependencies. Modern CPUs employ machine learning-based predictors that learn from past branch patterns to minimize misprediction rates [11], [13]. These predictors are often combined with *speculative pipelines*, where potential execution paths are evaluated in parallel.

Advanced prediction schemes such as two-level adaptive predictors and perceptron-based models significantly improve control flow accuracy [12]. Furthermore, hybrid designs integrate neural prediction networks that forecast pipeline stalls and data dependencies before they occur, enabling proactive hazard resolution.

4.6 Comparative Evaluation of Modern Implementations

Comparative analysis of recent architectures highlights a clear trend toward adaptability and hybrid optimization. Superscalar RISC-V pipelines outperform traditional scalar MIPS designs in both throughput and instruction latency. Meanwhile, adaptive-depth pipelines [13] and power-aware designs [5], [6] demonstrate the growing emphasis on balancing performance with energy efficiency.

Table-2: Comparison of Selected Pipelined CPU Architectures

Architecture	Pipeline Depth	Technique	Power Efficiency	Throughput Gain
MIPS 5-stage [9]	5	Basic forwarding	Moderate	Baseline
RISC-V (RV32I) [10]	5	Dynamic hazard detection	High	+15%
Superscalar OOO [11]	12–20	Tomasulo + speculation	Moderate	+40%
Adaptive-depth pipeline [13]	Variable	Depth reconfiguration	Very High	+25%
Low-power pipeline [6]	7	Resource-aware gating	Very High	+20%

4.7 Discussion

Optimization in instruction pipelining reflects a balance between complexity, energy efficiency, and execution speed. Superscalar and adaptive-depth pipelines continue to dominate high-performance designs, while low-power strategies enable efficient embedded implementations. The growing incorporation of AI-based predictive systems and modular ISA architectures like RISC-V signals the next stage of evolution in pipelined CPU design [15].

5. COMPARATIVE ANALYSIS AND DISCUSSION

Instruction pipelining has undergone a significant evolution from simple linear execution models to complex, dynamic, and adaptive architectures. The comparative analysis of modern pipelined CPU designs reveals that no single approach provides a universal solution to all performance, energy, and complexity challenges. Instead, optimization is achieved by integrating complementary techniques, tailored to the design goals and application domain.

5.1 Performance versus Complexity Trade-Offs

Early RISC-based pipelines emphasized simplicity and predictable performance. Classical five-stage designs, such as MIPS, offered clean instruction flows and efficient hardware utilization, but suffered from frequent stalls due to hazards [9]. Superscalar and out-of-order (OOO) execution models improved throughput by allowing multiple instructions to issue per cycle and by reordering execution dynamically. However, these gains came at the cost of increased hardware complexity, power usage, and verification difficulty [2], [11].

Recent studies, including those by Kim and Lee [5] and Wang and Li [6], demonstrate that performance scalability must be balanced against power and thermal constraints. High-performance superscalar processors often consume several times more power than simpler RISC pipelines, highlighting the necessity of power-aware and adaptive control mechanisms. Furthermore, deeper pipelines amplify branch misprediction penalties, making branch prediction accuracy a critical performance determinant.

5.2 Energy Efficiency and Power Optimization

Energy efficiency has emerged as a defining design criterion, especially in mobile and embedded systems. Techniques such as dynamic voltage scaling, clock gating, and operand isolation contribute to reducing energy waste in inactive pipeline stages [5]. Adaptive-depth and reconfigurable pipelines [13] further optimize energy consumption by selectively deactivating pipeline stages during low-load conditions.

Comparative analysis shows that low-power pipelines achieve up to 25% energy reduction while maintaining near-identical throughput compared to traditional fixed-depth designs [6]. These results underline that energy-aware design strategies are no longer secondary optimizations but integral to pipeline architecture planning.

5.3 Impact of ISA and Architectural Modularity

The choice of Instruction Set Architecture (ISA) significantly influences pipeline design flexibility. The open-source RISC-V platform allows designers to experiment with modular pipeline configurations, ranging from simple scalar pipelines to superscalar and speculative variants [10]. This modularity contrasts with legacy ISAs such as x86, which are constrained by backward compatibility requirements and rigid instruction formats.

RISC-V's five-stage baseline pipeline, as studied by Hossain and Rahman [10], demonstrates the advantages of clarity and adaptability. Moreover, its open framework fosters innovation in hazard handling and custom stage integration, making it a popular choice in both academic and industrial research [14].

5.4 Emerging Trends and Research Directions

The latest advancements in pipelining focus on incorporating intelligence and adaptability into CPU control logic. Machine learning-based branch predictors and AI-driven pipeline controllers have demonstrated promising results in reducing misprediction rates and optimizing stage utilization dynamically [12],[13]. These predictors leverage historical execution data and pattern recognition to anticipate hazards before they occur, allowing proactive mitigation.

Another emerging direction is the hybridization of pipelining with heterogeneous computing paradigms. Future CPUs are expected to feature configurable pipelines capable of adapting to specific workloads—balancing performance and power dynamically across AI, multimedia, and general-purpose tasks. Such hybrid architectures are also being extended into GPU and FPGA domains, enabling broader parallelism and workload-specific optimization.

5.5 Discussion Summary

The comparative review underscores three main insights are:

1. **Pipeline design is context-dependent:** High-throughput superscalar architectures suit performance-critical applications, while RISC-V and low-power pipelines fit embedded and energy-constrained environments.
2. **Adaptivity drives efficiency:** Dynamic reconfiguration and predictive control mechanisms are the key to balancing throughput and energy consumption.
3. **AI and automation are reshaping pipeline design:** Intelligent prediction and self-optimizing control units represent the future direction of CPU architecture research.

Overall, instruction pipelining continues to be a cornerstone of modern processor design. The transition from rigid, static architectures to flexible, adaptive, and intelligent systems marks a new era in CPU performance engineering.

6. FUTURE SCOPE

The concept of instruction pipelining continues to evolve as computing architectures advance toward higher complexity, heterogeneity, and efficiency. Future pipeline architectures are expected to move beyond static designs toward dynamically adaptive systems capable of reconfiguring themselves in real time according to workload behavior, thermal constraints, and power budgets. With the rise of machine learning-driven hardware optimization, predictive algorithms may play a crucial role in anticipating instruction dependencies and pipeline hazards before they occur, thereby minimizing stalls and improving parallelism. Moreover, as processors become increasingly specialized through domain-specific accelerators, hybrid pipeline designs that combine general-purpose and application-specific stages will likely become mainstream.

Emerging research also points toward the integration of artificial intelligence (AI) in the control logic of pipelined processors. Neural branch predictors and reinforcement learning-based schedulers can make pipeline execution more efficient and responsive under dynamic workloads.

Additionally, 3D-stacked architectures and chiplet-based CPUs provide an opportunity to shorten interconnect distances between pipeline stages, drastically reducing propagation delays and power dissipation. In the context of edge and embedded computing, lightweight and energy-aware pipelines will play a pivotal role in balancing performance with constrained resource environments. Future directions may also explore bio-inspired and quantum-inspired pipeline paradigms that draw from nontraditional computing principles to enhance throughput and scalability. As sustainability and energy efficiency become global priorities, the future of pipelining research will increasingly emphasize green computing, thermal-aware scheduling, and cross-layer co-design between hardware and software.

7. CONCLUSIONS

Instruction pipelining has remained one of the most enduring and transformative principles in CPU design, enabling modern processors to execute multiple instructions concurrently and efficiently. Through this review, a comprehensive analysis was carried out across different generations of pipelined architectures—spanning classical MIPS 5-stage processors, RISC-V pipelines, superscalar and out-of-order designs, and the latest adaptive-depth and power-optimized implementations. Each approach reflects a unique balance between speed, complexity, and efficiency, showcasing the progressive refinement of pipeline stages and control mechanisms over time. While hazards such as data, control, and structural conflicts continue to pose challenges, innovations in forwarding, dynamic scheduling, and speculative execution have significantly mitigated their impact.

Modern CPUs now integrate advanced techniques like dynamic voltage scaling, adaptive clocking, and deep learning-assisted hazard detection to achieve higher throughput with minimal energy cost. Furthermore, with the growing diversity of applications—from high-performance computing to low-power IoT devices—pipeline designs are increasingly being optimized for specific domains rather than general-purpose performance alone. The comparative review of existing architectures reveals that future trends will revolve around intelligent, power-efficient, and context-aware pipelines that can learn and adapt to runtime conditions. In conclusion, instruction pipelining continues to be not only a performance optimization but also a strategic architectural philosophy driving innovation in processor design. Its evolution will shape the next generation of computing systems that are faster, smarter, and more energy-conscious than ever before.

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