

Low-Depth Quantum Arithmetic Mapped to VLSI Reversible Gates

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Abstract— Low-depth quantum arithmetic is essential for reducing latency, decoherence, and power consumption in quantum and quantum-inspired computing systems. While CNOT and Toffoli gates are commonly used, alternative reversible gates can further optimize circuit depth, area, and energy efficiency when mapped to VLSI hardware. This work presents a VLSI-oriented realization of low-depth quantum arithmetic using Peres, Fredkin, and HNG gates. These gates enable compact arithmetic implementations by combining multiple logical functions within single reversible units, thereby reducing gate count and critical path length. The proposed approach maps low-depth quantum arithmetic operations such as addition and comparison onto CMOS-based reversible logic, ensuring minimal information loss and reduced switching activity. HDL-based simulation and synthesis results demonstrate improvements in depth, area, and power consumption compared to conventional CNOT/Toffoli-dominated designs. This work provides an efficient hardware mapping framework for quantum arithmetic suitable for quantum simulators, control electronics, and energy-efficient quantum-inspired accelerators. Further, hybrid reversible gate libraries combining Peres, Fredkin, and HNG gates with adiabatic CMOS techniques are devised to further minimize power dissipation. Optimizing gate selection based on arithmetic depth and switching activity can significantly reduce energy consumption while preserving computational accuracy, making the architecture suitable for low-power quantum control and edge-level quantum-inspired processors.

Keywords— Low-Depth Quantum Arithmetic, Reversible Logic, Peres Gate, Fredkin Gate, HNG Gate, VLSI Implementation, Quantum-Inspired Computing, Low-Power CMOS, Reversible Arithmetic Circuits, Energy-Efficient Hardware.

Introduction

Transistor scaling, performance optimization, and architectural parallelism have historically propelled the development of computing architectures. However, fundamental physical and thermodynamic constraints limit traditional scaling patterns as CMOS technology moves closer to deep sub-micron and nanoscale regimes. Leakage currents, heat density, interconnect parasitics, and dynamic switching power all work together to restrict additional performance improvements. Information loss is a fundamental aspect of computation in irreversible logic circuits. A direct correlation between information destruction and heat generation is established by Landauer's principle, which states that the erasure of one bit of information results in a minimum energy dissipation of $k T \ln(2)$. This thermodynamic limitation becomes more important as computing density rises.

A paradigm change is provided by reversible computation, which guarantees the bijective nature of logic transformations. Every output state in reversible logic uniquely predicts its corresponding input state, and the number of outputs and inputs is equal. Reversible circuits theoretically prevent bit erasure-induced energy dissipation because no information is erased. Under ideal physical conditions, conceptually reversible devices can approach arbitrarily low energy

consumption, as Bennett's extension of reversible computation showed. These ideas serve as the theoretical cornerstone of quantum computation, which requires unitary and intrinsically reversible processes.

Arithmetic operations account for a significant amount of circuit complexity in quantum computing. Addition, subtraction, and comparison blocks are essential to algorithms like Shor's factoring algorithm, quantum Fourier transform-based procedures, and modular arithmetic-intensive cryptographic computations. Computational fidelity and qubit decoherence likelihood are directly impacted by circuit depth. Reliability decreases as the number of gate layers grows due to increased noise exposure. Thus, in quantum architectures, arithmetic depth minimization is crucial.

Similarly, arithmetic circuits control dynamic switching power and propagation latency in traditional CMOS-based reversible implementations. In theory, reversible logic eliminates information-loss energy, but in practice, switching losses proportional to capacitive loading and transition frequency still occur in CMOS implementations. In CMOS devices, the dynamic power consumption is controlled by

$$P_{dynamic} = \alpha CV^2f$$

where f is the working frequency, V is the supply voltage, C is the effective capacitance, and α is the switching activity. Because there are many intermediate transitions, arithmetic circuits with deep cascaded gate topologies have significant switching activity. Consequently, switching energy and propagation delay are decreased when arithmetic depth is decreased.

Because of their universality and simplicity of synthesis, CNOT and Toffoli gates are widely used in traditional reversible arithmetic architectures. Universal gate sets make theoretical building easier, but they don't always give arithmetic functions structural efficiency. Long carry propagation chains, more garbage outputs, and a longer critical path latency are frequently the results of cascading universal gates. Arithmetic depth has not been consistently addressed as a fundamental optimization parameter in VLSI-oriented reversible design, despite the fact that the literature currently in publication places a strong emphasis on minimizing quantum cost and gate count.

The creation of a depth-aware reversible arithmetic mapping methodology is motivated by this. Multiple logical processes can be compressed into a single reversible unit by choosing reversible gates based on arithmetic functional density rather than universality alone. In order to create compact arithmetic structures that are ideal for CMOS-based VLSI implementation, this work presents a low-depth quantum arithmetic mapping framework that strategically uses Peres, Fredkin, and HNG gates. The suggested framework maintains computational correctness and logical reversibility while concurrently lowering circuit depth, switching activity, and propagation delay.

• literature survey

[1] Because they avoid information loss and allow computation to be reversed, reversible logic gates have drawn attention as a means of enabling low-power computing and opening up new possibilities for energy-efficient circuit design. Major reversible gates including Toffoli, Fredkin, HNG, and DKG are thoroughly examined in this paper, with an emphasis on their performance in terms of quantum cost, gate count, and real-world applications. According to the study, Toffoli gates work best for optimizing quantum circuits, whereas Fredkin gates perform very well in tasks involving data swapping and state management. The study promotes progress in VLSI design, cryptography, and quantum computing by combining cutting-edge advancements.[2] Reversible computing has become a viable way to deal with growing power dissipation in VLSI systems as CMOS scaling approaches its limits. In this work, a 32-bit Arithmetic Logic Unit is designed by substituting traditional AND and OR operations in a one-bit ALU framework with reversible logic gates like Toffoli, Fredkin, and Peres. Verilog is used to implement the design, while Xilinx ISE 14.7 and Model Sim Altera 6.3g are used to assess it. In comparison to irreversible ALU designs, the results demonstrate notable improvements, with an approximate 34% reduction in area and a 48.91% reduction in time.[3] Static, dynamic, short-circuit, and leakage components all contribute to power dissipation, which is still a significant problem in contemporary digital systems and drives the use of low-power strategies like reversible logic. Reversible gates are appropriate for energy-efficient VLSI architecture because they have zero heat dissipation and resource compatibility. A low-garbage reversible arithmetic and logical unit including adder, subtractor, and multiplier blocks is presented in this study along with a quantum cost and trash output analysis. The suggested architecture, which is implemented using Verilog HDL with synthesis and simulation in Xilinx tools, produces 11 garbage outputs and has a quantum cost of 57.[4] With applications in signal processing, nanotechnology, and encryption, reversible logic synthesis is essential for low-power design and quantum computing. The high size and power requirements of traditional secure algorithms are addressed by this work's proposal for a Reversible Logic Gates Cryptography Design (RLGCD). Using a Linear Feedback Shift Register to generate keys and Least Significant Bit

watermarking for further security, the architecture facilitates encryption and decryption. Evaluation of FPGA shows significant performance gains over conventional cryptography algorithms.[5] Reversible computing is widely applicable in CMOS, quantum computing, and QCA technologies and provides an efficient way to save area, cost, and power in VLSI design. In order to increase circuit efficiency, this study suggests a novel 3×3 SSG-I reversible gate that is multipurpose and universal in nature. The concept achieves a 38.77% increase in cost efficiency and performs better than current 3×3 reversible gates. Future uses of reversible logic in low-power and nanoscale systems are also covered in the study.[6] Reversible logic provides a practical method for creating low-power multipliers by reducing quantum cost, as power consumption has grown to be a crucial concern in contemporary VLSI design. This study maintains equal input-output lines while designing multipliers of different bit sizes utilizing reversible gates like Fredkin, Feynman, Peres, and Toffoli. Efficiency is assessed using a comparison study based on gate count, trash outputs, and quantum cost. Energy-efficient embedded applications can benefit from the suggested designs' optimized power performance.[7] Reversible logic gates are frequently utilized in low-power applications like optical computing and nanotechnology because they minimize heat dissipation in VLSI systems. Using reversible gates for encryption and decryption, this work introduces an image cryptography technique based on Reversible Logic Gates Cryptography Design (RLGCD). For key generation, a Reversible Linear Feedback Shift Register is employed, which offers more power efficiency than traditional LFSR designs. Secure encryption with reduced image distortion and improved energy performance is demonstrated by implementation in MATLAB and Xilinx Vivado.[8] Multipliers are a crucial part of VLSI arithmetic units, and reversible logic has become crucial for lowering energy consumption and enabling fault-tolerant and quantum computing systems. The main goal of this research is to construct different reversible multiplier architectures and assess their functionality and efficiency. Parameters including the number of gates, garbage outputs, constant inputs, quantum cost, delay, depth, and overall cost are used to examine the suggested designs. A comparison with previous research reveals the benefits and drawbacks of several reversible multiplier techniques.[9] A fast 16x16 Dadda multiplier that is optimized for FPGA implementation using Verilog in Xilinx Vivado 2018 is shown in this study.3. In comparison to traditional array multipliers, the Dadda reduction algorithm achieves lower hardware complexity and delay by minimizing partial products. Efficiency is further increased by integrating reversible logic gates, which lower resource and power consumption. According to experimental data, the design is appropriate for real-time DSP and embedded applications with a latency of 4.638 ns and a power consumption of 0.474W.[10] The usage of Distributed Quantum Computing with Residue Number System-based modulo adders is motivated by the limitations of quantum arithmetic in the NISQ era, which include noise and restricted qubit resources. This study presents a new Quantum Diminished 1 Modulo (2^n+1) Adder design and the QSMART tool for creating optimized RNS quantum adders taking depth, range, and efficiency into account. According to simulations using Quantum HI ion-trap models, distributed RNS addition outperforms non-distributed adders in terms of output probability by 11.36% to 133.15%. Beyond the limitations of present 20-qubit hardware, the method allows scalable quantum addition.[11] Though finite field inversion, which is essential for algorithms like Shor's solution to the ECDLP, has not received enough attention, research on quantum cryptanalysis has grown quickly. By using a waterfall translation of the Itoh-Tsujii method and doing away with inverse squaring operations, this approach decreases the depth of quantum inversion based on Fermat's Little Theorem. The method reduces the number of CNOTs and the depth of the circuit, and it has been verified by complete implementation and resource analysis in Qiskit. Gidney's relative-phase Toffoli gate, which offers a quicker substitute for quantum inversion, is used to obtain additional advantages.[12] Although qudit systems are advantageous for error correction and multi-phase computation, NISQ devices have not yet fully explored useful multi-qudit operations like quantum addition. With the introduction of a library of quaternary gates and optimized quaternary complete adders with lower depth and T-gate consumption, this study offers the first technique for quaternary quantum addition utilizing primitive gates. When compared to baseline designs, implementations in IBM Qiskit show reductions of up to 1.4× T-depth and 1.7× T-count. Carry-ripple adders, which achieve 1.4× greater fidelity in noisy environments, are used to validate scalability.[13] Practical quantum algorithms require quantum addition circuits, but NISQ devices cannot handle the overhead of completely fault-tolerant designs, which encourages the use of low-depth alternatives. An out-of-place Quantum Carry Lookahead Adder based on Clifford+T gates is presented in this study; its main goal is to minimize the expensive use of T-gates. To further reduce T-count while preserving compatibility with upcoming fault-tolerant architectures, a unique uncomputation technique is presented. Bilinear interpolation is used in a quantum image processing application to illustrate how the suggested architecture performs better than current adders in terms of overall gate cost.[14] Ultrasonic guided waves are a promising medium for mechanical communication channels because they can propagate over large distances with little attenuation. This study creates a guided-wave communication system that uses channel reciprocity to reduce reciprocal interference between transducers, multipath fading, and reverberation. For compatibility with inexpensive switching amplifiers, a unique technique that combines the Time-Reversal method with low-depth synthesis of time-reversed waveforms is put forth. Reliable communication speeds up to tens of kHz without information loss are demonstrated in simulations conducted on metal panels.[15] Sparse data processing is made more difficult by the geographical locality limits imposed by modern accelerator architectures, where the cost of transmission is

dependent on physical distance. In order to optimize processor locality using a unique tree layout method, this work presents a framework for spatial tree algorithms within the spatial computer model. The suggested solution allows for effective locality-aware messaging while achieving polynomial energy improvements over PRAM-style techniques. With high probability, the resulting tree sum and lowest common ancestor algorithms achieve poly-logarithmic depth and near-linear energy.[16] Although noise and restricted scalability limit the application of QAOA to big problems, it provides a strong method for combinatorial optimization. In order to provide low-depth, high-quality solutions, this work presents a quick hybrid multilevel framework that parameterizes QAOA across hierarchy levels and reinforces it with genetic algorithms. It is demonstrated that relaxation-based coarsening maintains structural information necessary for efficient QAOA optimization by transferring parameters from course to fine levels. The outcomes show that multilayer QAOA has the potential to be a scalable solution for near-term quantum devices.

• Existing Algorithm

The current approaches to reversible arithmetic design, as covered in mostly concentrate on building logic circuits with basic reversible gate libraries including CNOT, Toffoli, Fredkin, and Peres gates, as well as a few higher-dimensional arithmetic-oriented gates like HNG, DKG, TSG, and MRG. These designs prioritize garbage output minimization, quantum cost reduction, and functional correctness. Nevertheless, arithmetic circuits typically still have a cascade-dominant structural organization, which results in deeper circuits.

Because of its universality, the Toffoli gate is frequently utilized in conventional reversible full adder implementations. The carry output of each stage feeds into the subsequent stage, and the carry signal is produced using a standard Toffoli-based ripple-carry adder using controlled-controlled processes. A strictly sequential dependency chain is produced as a result. The depth complexity of an n-bit addition is proportional to the operand width since the carry needs to travel across n cascaded gate levels. Despite the possibility of optimizing quantum cost through meticulous decomposition, carry propagation delay keeps the critical route lengthy.

Signal duplication and parity preservation are two common uses for the CNOT gate. However, reversible logic requires additional gates to copy signals because direct fan-out is prohibited. This raises the number of intermediate transitions and gates even further. In CMOS-based implementations, these actions provide more logic levels and switching activity while maintaining reversibility.

Because the Peres gate integrates AND and XOR capabilities into a single transition, it has been utilized to lower quantum cost in arithmetic circuits. This lowers the gate count in half-adder implementation when compared to independent Toffoli and CNOT structures. Nevertheless, Peres gates are locally added without altering the global carry propagation design in a large number of documented implementations. As a result, overall depth reduction is still constrained.

Because they concurrently provide sum and carry outputs, higher-dimensional gates like HNG and DKG allow for more compact full adder implementations. However, the literature now in publication usually portrays these gates as discrete enhancements rather than elements of an all-encompassing depth-optimization approach. Linear depth scaling is achieved in ripple-based arithmetic circuits because the sequential carry chain is unaffected even if each stage is compact.

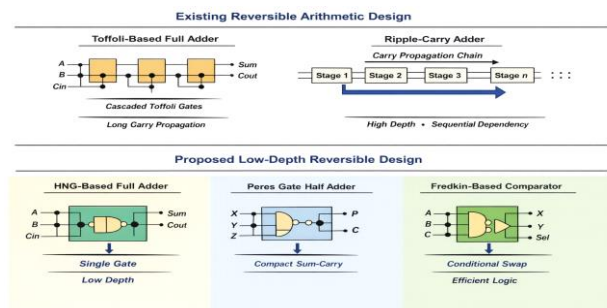


Fig 1:Existing Reversible Arithmetic Design

- The current design features a ripple-carry structure and a full adder based on Toffoli. The sum and carry outputs of the Toffoli-based complete adder are produced by cascading Toffoli gates. The carry signal spreads stage by stage as a result of several gates being connected in succession. High circuit depth and severe sequential dependency are the results of this extended carry propagation chain. Higher latency and more switching activity result from the depth increasing linearly with the number of bits.

Furthermore, the majority of current research analyzes reversible circuits using static criteria such as garbage outputs, gate count, and quantum cost. Despite their significance, these measures fall short in describing hardware-level performance in CMOS-based implementations. Although switching behavior and propagation delay are directly impacted by circuit depth, depth is rarely considered the main optimization goal. Dynamic power consumption is increased when transitions are switched across several cascaded stages, particularly in workloads that are mostly arithmetic-based.

Sequential control dependencies are also present in arithmetic logic units and comparator circuits built with Fredkin and Toffoli gates. Cascaded control structures are frequently used to implement conditional operations, increasing the logic depth. While some architectures prioritize fault tolerance and parity preservation, the effect of successive layering on switching energy is not thoroughly investigated. Therefore, structural organization rather than functional competence is the main drawback of current reversible arithmetic approaches. When operand size rises, cascaded architectures with universal gate dominance scale poorly in depth. Both quantum and CMOS-based reversible systems function less well when a systematic depth-minimization technique is not used.

• Proposed Algorithm

For CMOS-based VLSI implementation, the suggested architecture presents a structured depth-optimized reversible arithmetic mapping mechanism. The main goal is to reduce the depth of the arithmetic circuit while maintaining computational accuracy and logical reversibility. The suggested method chooses reversible gates according to arithmetic functional density, allowing several logical operations to be incorporated within a single reversible transformation step, in contrast to traditional reversible arithmetic designs that promote universal gate decomposition.

The maximum number of successive gate layers encountered along any signal path from primary input to primary output is the formal definition of depth in reversible arithmetic circuits. A subset of the circuit's L reversible gate layers should be traversed by each signal path. The maximum path length for each input-output pair is the arithmetic depth D . In quantum systems, when the length of circuit execution is constrained by the decoherence time, minimizing D directly lowers the propagation delay and sequential dependency.

Arithmetic blocks are rearranged into compact reversible primitives in the suggested architecture. The main component needed to realize a full adder is the HNG gate. Several cascaded control procedures are used in traditional Toffoli-based implementations to generate the sum and carry outputs. Sequential dependency is introduced at each level, and depth increases linearly with operand size. On the other hand, the HNG gate combines AND-based carry generation and XOR-based sum computation into a single reversible mapping. The HNG gate lowers per-bit arithmetic depth to a single transformation stage by producing both outputs at the same time.

Likewise, the Peres gate is used to calculate intermediate carry signals and partial sums in early-stage arithmetic processes. The Peres gate's transformation is appropriate for half-adder and carry-merge functionality since it naturally integrates XOR and AND behavior. Intermediate carry-only logic levels are removed by integrating both operations into a single gate. As a result, fewer cascaded stages are needed overall for addition.

To reduce sequential reliance, the carry propagation mechanism is redesigned. The suggested architecture compresses carry computation within multifunctional gates as an alternative to depending on strictly linear ripple-carry propagation. The architecture reduces the physical gate layers while maintaining logical ripple reliance for correctness. As a result, even when operand width rises, the maximum sequential gate depth drops. As a result, in contrast to conventional Toffoli-dominated ripple topologies, the effective critical path latency increases more slowly.

Three compact arithmetic blocks are depicted in the suggested design: a Fredkin-based comparator, a Peres gate half adder, and an HNG-based full adder. The HNG gate reduces the number of cascaded stages by generating sum and carry in a single reversible construction. By combining XOR and AND operations, the Peres gate allows for the creation of compact sum-carries using fewer logic levels. By carrying out conditional swap operations, the Fredkin gate reduces

control depth and streamlines comparator logic. This section emphasizes that, in comparison to the current cascaded structure, the suggested design achieves lower depth, fewer sequential steps, and more effective arithmetic mapping.

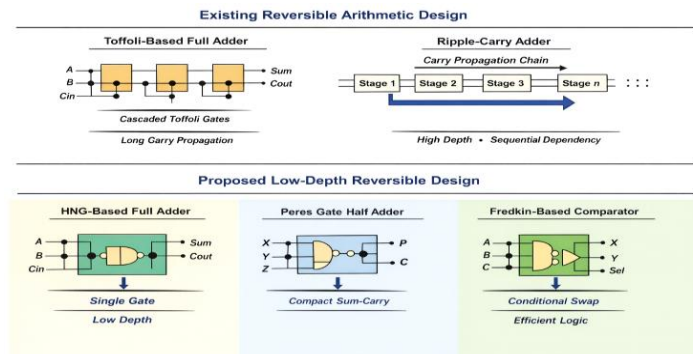


Fig 2:Proposed Low-depth Reversible Design

The Fredkin gate is used to implement controlled swap functionality for comparison and conditional selection procedures. Multiple cascaded control gates are frequently needed for conditional logic in traditional reversible comparators. The comparator depth is decreased by directly employing controlled swap operations. The Fredkin gate compresses the depth of control logic by enabling routing decisions without adding additional multiplexing steps.

There are several advantages to depth reduction from the standpoint of VLSI mapping. In CMOS implementation, each reversible gate layer is equivalent to a network of transistors. Transistor stacking and parasitic capacitance accumulation are increased by cascaded gate layers. The suggested architecture reduces effective capacitive loading along the critical path by lowering the number of successive layers. This enhances signal integrity and lowers propagation delay. Depth also has a big impact on switching activity. Intermediate signals in cascaded systems may toggle even when the end outputs don't change, which adds needless dynamic power dissipation. There are fewer intermediate switching nodes when arithmetic operations are embedded into single reversible units. This directly lowers energy consumption since dynamic power in CMOS circuits is proportional to switching activity. Reduced depth also improves stability in high-frequency operation by lowering the likelihood of glitch propagation.

A depth-aware gate selection technique is also included in the suggested architecture for mapping. The mapping framework recognizes arithmetic patterns like half-adder, full-adder, and conditional routing blocks and allocates them to Peres, HNG, or Fredkin gates appropriately, rather than breaking down Boolean arithmetic operations only into universal gates. Gate selection is guaranteed to be in line with depth minimization goals and arithmetic functionality thanks to this organized mapping.

Scalability is a crucial factor to take into account. As the operand width increases, depth in traditional ripple-based reversible adders scales linearly. In the proposed design, although logical dependency remains, the compression of arithmetic operations within each stage reduces effective depth scaling. This leads to quantifiable gains in switching energy and delay for large operand sizes. Therefore, as mathematical complexity increases, the architecture gains more and more benefits.

Additionally, hybrid integration with adiabatic CMOS logic is supported by the suggested framework. By recycling charge throughout logic transitions, adiabatic approaches lower physical switching losses while reversible logic lowers information-loss energy. A dual-layer approach to energy reduction is produced by combining adiabatic switching with depth-optimized reversible gates. Practical dynamic power dissipation is minimized by adiabatic implementation, and theoretical entropy buildup is minimized by logical reversibility. The design is generated using CMOS technology libraries and modelled in HDL to verify performance gains. In comparison to traditional CNOT/Toffoli-based architectures, critical path delay, gate count, area usage, and power consumption are extracted. The evaluation framework provides a thorough performance assessment by measuring both hardware-level switching behaviour and quantum cost equivalency.

All things considered, the suggested design creates a methodical, arithmetic-focused reversible mapping approach that specifically focuses on VLSI efficiency and depth minimization. The design delivers lower switching activity, higher scalability, increased energy efficiency, and decreased critical route delay by choosing Peres, HNG, and Fredkin gates according to their arithmetic functionality and switching behavior. Because of this, the architecture is especially well-suited for low-power quantum-inspired computers, quantum simulators, quantum control circuits, and cryptographic accelerators.

• **Results And Discussion**

The designs are developed in Xilinx Vivado tool for the hardware of choice is 28nm CMOS technology based Artix-7 FPGA board (xc7z020clg484-1). The system requirements include windows 10 OS, 4 GB RAM installed with Xilinx Vivado 2023.2. The simulation result of existing and proposed designs are as shown in fig. 3(a) & 3(b).

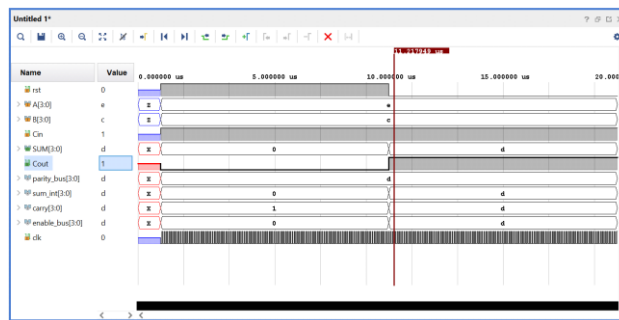


Fig 3(a): Simulation result of Existing Design



Fig 3(b): Simulation result of Proposed Design

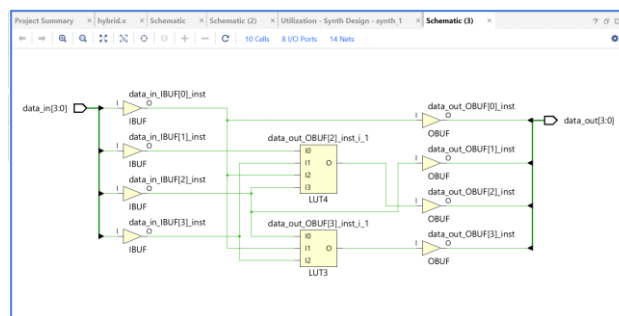


Fig 4(a): Technology Schematic of Existing design

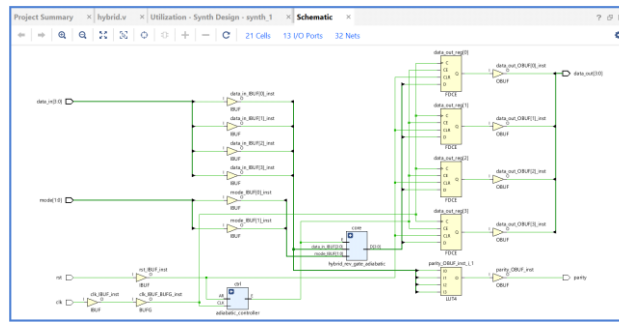


Fig 4(b): Technology Schematic of Proposed design

- The technology schematics of existing and proposed designs are shown in fig.4 (a) and (b) respectively.
- The circuit uses 10 logic cells, 8 I/O ports, and 14 nets, according to the technological diagram of the current design created in Xilinx Vivado. Four input buffers (IBUFs) connect the input signals, and four output buffers (OBUFs) drive the outputs. LUT3 and LUT4 blocks, which realize the combinational logic obtained from traditional reversible gate operations, are used to implement the arithmetic logic. Several LUT stages are used in this approach to carry out the arithmetic operations. According to the technology diagram of the suggested design, the circuit makes use of 32 nets, 13 I/O ports, and 21 logic cells. IBUFs are used to connect inputs such as data, clock, reset, and mode signals, while a BUFG global clock buffer is used to distribute the clock. LUT-based logic blocks are used to implement reversible arithmetic operations based on Peres, Fredkin, and HNG gates. OBUFs provide a more comprehensive and effective architecture for reversible arithmetic implementation by driving the outputs, which include data and parity signals.
- According to the comparison results, the suggested reversible gate architecture outperforms the current design in terms of performance. A lower arithmetic depth is shown by the maximum propagation delay being lowered from 7.029 ns to 6.935 ns. Additionally, there is an improvement in energy efficiency as the overall on-chip power usage drops from 1.605 W to 1.278 W. Additionally, the junction temperature drops from 43.5 °C to 39.7 °C, indicating improved thermal properties. These enhancements confirm that the suggested reversible arithmetic architecture based on Peres-Fredkin-HNG offers a more effective VLSI implementation appropriate for low-power quantum-inspired computing systems.

Table 1:comparison among existing and proposed designs

Parameter	Existing Design	Proposed Design
Maximum Total Delay (ns)	7.29	6.935 ns
Logic Delay (ns)	3.848	3.636 ns
Net Delay (ns)	3.181	3.299 ns
Minimum Hold Delay (ns)	1.647	0.372 ns
Total On-Chip Power	1.605	1.278 W
Dynamic Power	1.472 W	
Static Power	1.133	0.125 W
Signal Power	1.28	0.090 W
Logic Power	1.08	0.071 W

I/O Power	1.436	0.991 W
Junction Temperature	43.5 °C	39.7 °C

Conclusion

In this paper, a VLSI implementation of reversible gates for low-depth quantum arithmetic was provided. To obtain a more effective arithmetic realization, the suggested architecture makes use of Peres, Fredkin, and HNG gates rather than traditional CNOT and Toffoli gates. The suggested architecture lowers the propagation latency from 7.029 ns to 6.935 ns, the total on-chip power from 1.605 W to 1.278 W, and the junction temperature to 39.7 °C, according to implementation results in Xilinx Vivado. These enhancements show that the suggested reversible logic design offers a more effective and energy-efficient solution for VLSI arithmetic systems inspired by quantum mechanics. In order to further minimize power consumption for scalable quantum and edge computing hardware, future work can extend this design to complicated arithmetic units like multipliers and ALUs and investigate adiabatic CMOS and sophisticated reversible gate libraries.

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