VLSI implementation of Toffoli /CNOT based quantum Circuits

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Abstract *— The rapid advancement of quantum computing has increased the need for efficient classical hardware support for quantum circuit realization, control, and simulation. Among quantum logic primitives, the Controlled-NOT (CNOT) and Toffoli (CCNOT) gates play a fundamental role in quantum algorithms, reversible computing, and quantum error correction. This work presents a VLSI implementation of CNOT- and Toffoli-based quantum circuits using synthesizable Verilog HDL, enabling compatibility with both FPGA and ASIC design flows. The proposed architecture maps quantum reversible operations into classical CMOS logic using XOR and AND–XOR realizations while preserving reversibility and minimizing information loss. Functional verification is performed through logic simulation, and synthesis results demonstrate low area overhead and reduced power consumption compared to conventional irreversible logic designs. The presented implementation provides a scalable and technology-independent framework suitable for quantum circuit emulation, quantum control electronics, and quantum-inspired accelerators, thereby bridging the gap between abstract quantum logic and practical VLSI hardware realization. Further the work is extended for multi-controlled Toffoli gates-based fault tolerant reversible architectures such as reversible D flipflop.*

Keywords- CNOT Gate, Low-Power CMOS, Quantum-Inspired Hardware, Reversible Logic, Toffoli Gate, VLSI Implementation.

1. Introduction

With exponential or polynomial speedups over classical counterparts, quantum computing has become a breakthrough computational paradigm that can solve specific kinds of problems. Quantum algorithms provide benefits in large-scale arithmetic processing, optimization, quantum system simulation, and cryptography by taking advantage of quantum mechanical concepts including superposition, entanglement, and interference. However, technological constraints such as limited qubit connectivity, gate fidelity degradation, decoherence, and limited coherence duration in Noisy Intermediate-Scale Quantum (NISQ) devices continue to impede the practical implementation of quantum circuits. Because of these limitations, quantum circuits must be carefully optimized before being implemented on hardware platforms.

The Controlled-NOT (CNOT) and Toffoli (CCNOT) gates are two of the few universal reversible logic primitives that are at the heart of the majority of quantum algorithms. As the basic two-qubit entangling operation, the CNOT gate finds extensive application in arithmetic circuits, state preparation procedures, and quantum error correction. By flipping a target qubit only when many control qubits meet a predetermined condition, the Toffoli gate—also known as the controlled-controlled-NOT gate—expands conditional logic. Crucially, every classical Boolean function may be built from a network of Toffoli gates since the Toffoli gate is universal for reversible Boolean processing. Because of this characteristic, it is essential to both reversible classical structures and quantum computers.

The optimization of layout mapping and quantum logic synthesis has been the main focus of recent research efforts. Multi-controlled Toffoli gates must be broken down into single-qubit and two-qubit gates, primarily CNOT gates, in order to be directly run in quantum hardware. Additionally, additional SWAP operations are frequently needed to bring non-adjacent qubits closer together because to restricted qubit connectivity, which greatly increases circuit depth and error probability. Advanced layout synthesis techniques co-optimize qubit mapping and gate decomposition in an effort to reduce these overheads. Although these methods increase the efficiency of execution on quantum processors, they do not address transistor-level implementation and instead concentrate on abstract gate changes.

Reversible logic circuits and quantum-inspired classical computing architectures are gaining popularity at the same time as quantum hardware. Each piece of information lost in irreversible computation loses a minimal amount of energy proportional to thermal noise, according to Landauer's principle. By guaranteeing bijective input-output mapping, reversible circuits prevent information loss and, in theory, lower energy dissipation. This idea drives the creation of reversible gate classical CMOS implementations like CNOT and Toffoli, which can be used as building blocks for quantum control electronics, low-power CPUs, and cryptographic accelerators.

Comprehensive VLSI frameworks that convert quantum logic primitives into scalable CMOS designs are still scarce, despite the fundamental significance of reversible gates. There is a gap between the abstraction of quantum circuits and their physical hardware realization because most of the current work focuses on either high-level reversible logic theory or quantum compilation approaches. By suggesting a synthesizable VLSI design for CNOT and Toffoli-based circuits, together with enhancements toward multi-controlled topologies and reversible sequential elements, the current study fills this gap. The goal is to create a link between realistic FPGA/ASIC implementations and quantum logic synthesis techniques so that reversible hardware systems can be realized effectively.

2. Literature survey

[1] By concentrating primarily on meeting hardware restrictions for CNOT gates, state-of-the-art quantum layout synthesis techniques simplify the challenge by assuming that circuits only contain single- and two-qubit gates. However, multi-controlled Toffoli (MCT) gates are commonly used in practical quantum circuit design, and their direct decomposition using preset routines overlooks optimization opportunities from other logic synthesis approaches. By first breaking down MCT gates into Toffoli gates and then establishing an effective qubit-mapping verification procedure for SWAP-free layout creation, this study suggests a co-optimization framework that simultaneously carries out quantum logic and layout synthesis. The approach takes into account both decomposition and SWAP overheads to reduce total cost when SWAP-free solutions are not practical. Experimental results provide a roughly 25× runtime gain over current methods and a 16% decrease in additional CNOT gates.[2] For scalable quantum implementation, multi-bit Toffoli gates—essential parts of quantum algorithms—must be effectively broken down into elementary gates like CNOT, T, and Hadamard. Using two optimization models and closed-form solutions for optimal decomposition, this work suggests a workable engineering approach for creating multi-bit Toffoli gates. The models use linearized multi-objective integer programming, taking into account variables like available basis gates, ancilla states, and target ancilla count. The suggested method shows efficacy for noisy intermediate-scale quantum environments with a variety of hardware specifications by methodically addressing hardware limitations such as qubit availability and circuit depth.[3] In contrast to current heuristic approaches that need an average of 9.29 gates, this study shows for the first time that any 4-input Boolean function may be achieved with a maximum of five Toffoli gates. The outcome is useful for quantum Boolean circuit design frameworks based on LUT-network synthesis, both conceptually and practically. Complex Toffoli gates are a novel concept that was introduced because traditional SAT-based exact design methodologies are unable to establish the true minimum gate count. This idea effectively formulates the problem as an SMT model, significantly narrowing the search space for the best way to synthesize quantum circuits.[4] Applications in cryptanalysis, image processing, and secure communication are made possible by quantum modular adders, which are crucial building blocks for complex quantum operations like subtraction and multiplication. Four architectures that simultaneously compute regular and modulo sums for residue number system arithmetic are shown in this paper, which presents the earliest known designs of quantum modulo (2^n+1) adders. Through gate optimization and zero-reset approaches, the suggested designs gradually improve performance while achieving notable decreases in CNOT count and depth, Toffoli usage, and qubit requirements. Up to 28.8% error reduction is shown in experiments on the 127-qubit IBM Washington processor, confirming the suggested adders' usefulness.[5] Although cryptanalysis and quantum computing research has expanded quickly, little is known about finite field inversion, which is essential for algorithms like Shor's solution to the Elliptic Curve Discrete Logarithm Problem. This work eliminates inverse squaring operations and adopts a full waterfall translation of the Itoh–Tsujii approach to minimize the depth of existing quantum inversion circuits based on Fermat's Little Theorem. Implementation and resource analysis in the Qiskit simulation environment confirm that the suggested design reduces the number of CNOT gates and circuit depth. A more time-efficient quantum inversion architecture is made possible by employing Gidney's relative-phase Toffoli gate, which yields further advancements.[6] Since adders are essential to processor speed, reversible computing has drawn interest for its potential to lower power consumption and heat dissipation. Reversible Toffoli gates are used in place of traditional look-ahead logic in the suggested architecture,

which also incorporates a hybrid variable-latency extension to reduce energy consumption without appreciably reducing speed. Reversible circuits are useful in low-power VLSI systems, photonic computing, and nanotechnology because they maintain an equal number of inputs and outputs. In comparison to current designs, the proposed reversible carry look-ahead adder exhibits lower trash outputs, fewer gates, and better quantum efficiency. [7] Quantum dot cellular automata (QCA) have become a viable substitute for CMOS technology as it gets closer to physical scaling limits for nanoscale computing. In addition to allowing the development of reversible logic circuits that circumvent the energy dissipation seen in traditional gates, QCA has benefits like high packing density, low power consumption, and faster operation. With just 14 cells taking up 0.02 μm^2, this work proposes a revolutionary Toffoli gate architecture that explores the construction of power- and area-efficient reversible logic utilizing QCA. Improved functionality and efficiency are confirmed by simulation using QCA Designer 2.0.3, which qualifies the design for use in upcoming nanoscale integrated circuit applications.[8] Though efficient quantum circuit designs with reduced qubit count, gate count, and depth are necessary for practical adoption, large-scale quantum computers hold the potential of solving challenges beyond the scope of classical computing. The fundamental function $f_k(S) = \max(S-K, 0)$ is implemented and optimized as a quantum circuit for financial applications in this work to address quantum option pricing. Using strategies like parallelization, qubit reuse, and optimal adder selection, a number of efficient designs are created while taking trade-offs between qubit utilization and circuit depth into account. To accommodate a range of application needs, several circuit variations with various adder configurations and Toffoli decompositions are offered.[9] Since even 4-bit reversible functions give 16! possibilities, it is difficult to synthesize reversible functions optimally due to the vast search space, which requires more than 100 terabytes to store all Toffoli-based implementations. In order to make the challenge computationally feasible, this paper describes two algorithms that produce an optimal circuit for each 4-bit reversible specification and list all optimal implementations. In order to determine the toughest instances and examine the distribution of ideal solutions, extensive experiments are carried out on benchmark functions, random permutations, and linear circuits. The method is further expanded to include physical restrictions like LNN architecture, proving its applicability to heuristic evaluation and quantum circuit design.[10] By utilizing quantum mechanical principles, quantum computing provides a new paradigm for problem-solving that goes beyond what is possible with classical methods. Based on a complete adder built with CNOT and CCNOT gates, this work suggests low quantum-cost adder architectures that can be used to create parallel and carry select adders. The carry select adder uses CSWAP gates, which are modeled as 2×1 multiplexers, to choose outputs from parallel adders, whereas the parallel adder doesn't need any extra gates. The IBM Qiskit framework is used to analyze performance indicators during the design and evaluation of every circuit.[11] Powerful algorithms like Grover's search and Shor's factorization are made possible by quantum computing, which uses superposition, entanglement, and interference to reach exponential parallelism beyond classical processing. Scalability, coherence, and error correction are issues that several physical platforms, such as superconducting, photonic, spin-based, and trapped-ion systems, must deal with. Applications in artificial intelligence, optimization, drug discovery, and cryptography are being accelerated by developments in cloud computing and hybrid quantum-classical models. Quantum computing is continuing to advance toward revolutionary real-world effects through ongoing research on fault tolerance and qubit scaling.[12] Practical circuit synthesis is hampered by the Nearest Neighbor Architecture's (NNA) restriction of quantum operations to nearby qubits. An SMT-solver-based approach to creating quantum circuits with CNOT, H, and T gates that completely satisfies the NNA constraint is shown in this study. In contrast to current SMT methods, the suggested method optimizes CNOT use by taking advantage of "Don't Care" circumstances at intermediate stages and directly handling H and T gate functionality. Comparing experimental evaluation to traditional approaches that disregard these constraints, the average reduction of CNOT gates is 58.11%.[13] A vertically symmetric Fin-based architecture is proposed in this study to achieve high-fidelity CNOT gate operations with a small device footprint. Fine tuning of qubit states is made possible by a surrounding mid-gate, while the tunnel coupling and exchange interaction are efficiently regulated by designing the high-k oxide and interlayer thickness. The design achieves a CNOT operating time of 45.3 ns under a gradient magnetic field, which is similar to top semiconductor implementations. A gate fidelity of 99.81% is demonstrated by noise analysis taking into account 1/f and Lorentzian spectra, suggesting a scalable CMOS-compatible method for silicon quantum processors.[14] In this research, we propose an exact SMT-based approach to minimize noisy CNOT utilization while synthesizing CNOT networks that comply with the Nearest Neighbor Architecture on 2-D quantum devices. The suggested method, in contrast to earlier methods, permits variable T-gate relocation, allowing for better optimization and more freedom in the placement of surrounding logic. In order to loosen reliance on T-gate positions and generate circuits more efficiently, new constraint formulations are presented. The solution delivers 58.11% lower quantum cost and 29.22% runtime reduction when compared to Ding et al. and IBM Sabre

Swap.[15] This research suggests a paradigm for safe delegated quantum computing that combines the Quantum One-Time Pad with the Quantum Approximate Optimization Algorithm to tackle optimization problems like MAX-CUT while maintaining data confidentiality. Using randomly generated keys, the client prepares and encrypts the initial quantum state before sending it to the cloud server for processing. Without gaining access to private data, the server carries out the necessary quantum operations. The client then decrypts and measures the outcome to get an approximate solution. For cloud-based quantum services, the method combines robust security guarantees with quantum optimization capabilities.[16] Limited qubit counts and gate fidelity limit the scalability of quantum circuits in the NISQ era, and current synthesis techniques frequently overlook the spatial structure of Boolean functions. In order to improve optimization and lower circuit complexity, this work presents Spatial Structure-based Hypercube Reduction (SSHR), which takes advantage of parallelotope properties in the Boolean hypercube. Two variations are suggested: SSHR-I, which uses integer linear programming for deeper structural exploitation, and SSHR-H, which uses quick heuristic synthesis. By lowering CNOT counts by 56% and 81%, respectively, the strategy outperforms ESOP and XAG techniques.[17] Despite its significance in quantum optimization, the efficiency of entanglement and state preparation in Variational Quantum Eigensolver (VQE) circuits is still unknown. This study examines the effects of CNOT-based entanglement and Hadamard initialization by evaluating eight circuit designs on 100 randomly generated MaxCut tasks. The findings show that while entanglement frequently lowers solution quality, especially as circuit depth grows, initial Hadamard gates offer little performance improvement. These results point to important areas for the development of hybrid algorithms in the future by indicating that entanglement may have a coordinating function that can be harmful when abused.

3. Existing Design

Instead of treating layout synthesis and logic synthesis as separate steps, state-of-the-art research in quantum circuit optimization has increasingly acknowledged the significance of taking both into account together. Layout Synthesis for Quantum Circuits Considering Toffoli Gate Decomposition is the reference study, offers a co-optimization approach that combines qubit mapping and Toffoli gate decomposition techniques while taking hardware connectivity limitations into account.

Toffoli Gate Definition

In traditional quantum compilation procedures, layout synthesis is used to allocate logical qubits to physical qubits on the target device after multi-controlled Toffoli (MCT) gates are first broken down into single- and two-qubit gates according to a preset strategy. On the other hand, different decomposition decisions result in unique interaction graphs, which have a direct impact on routing complexity. According to the reference study, when connectivity constraints are applied, a fixed decomposition technique may yield less-than-ideal outcomes. The authors present a versatile method that concurrently takes into account several decomposition options during mapping in order to solve this problem.

Two main decomposition techniques for the 2-controlled Toffoli gate are examined. The first technique, which is also known as the C-type decomposition, creates a triangle interaction pattern between three qubits using six CNOT gates. When three-clique connection is supported by the destination hardware, this design works well; but, if it is not, additional SWAP gates can be needed. The second technique, called the V-type decomposition, uses a linear chain topology with eight CNOT gates. Its linear structure makes it easier to align with normal coupling graphs, which may reduce SWAP insertion, even though it adds a greater intrinsic CNOT count.

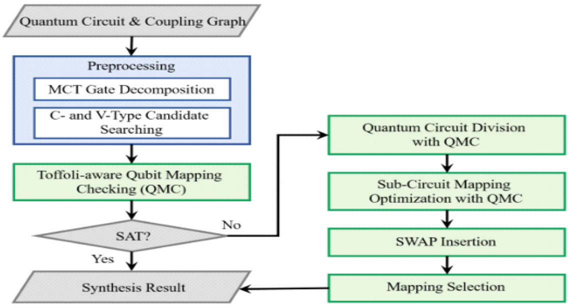


Fig 1: The overall flow of Existing Design

The analysis in the reference publication is expanded to include multi-controlled Toffoli gates. These gates must be broken down into networks of Toffoli gates utilizing supplementary qubits because gates with more than two controls cannot be directly executed by present quantum hardware. There is discussion of both clean and dirty ancilla methods. While filthy ancilla decomposition lowers qubit utilization at the cost of greater circuit depth, clean ancilla decomposition minimizes gate count but demands more qubit resources. The overall cost and mapping flexibility are directly impacted by the breakdown approach chosen.

The reference work formulates the mapping problem as an instance of Satisfiability Modulo Theories (SMT) to find the best qubit placements. This formulation dynamically chooses between C-type and V-type decompositions, guarantees that logical qubits are assigned to different physical qubits, and includes nearest-neighbour constraints. The SMT solver instantly detects a complete SWAP-free mapping solution if one exists. In the absence of this, the circuit is split up into maximally SWAP-free sub-circuits, and cost functions that take into consideration CNOT and SWAP overhead are used to build optimal transitions between sub-circuits.

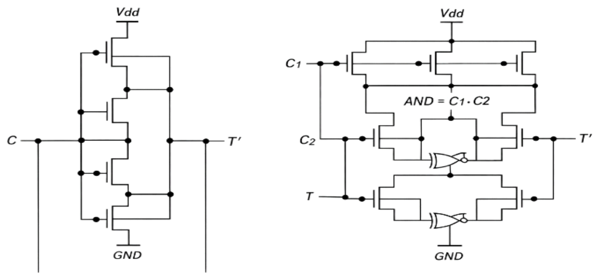
During SWAP insertion, an improved gain function is added to avoid endless routing loops. Furthermore, the mapping configuration that minimizes the overall CNOT cost—including both decomposition and routing overhead—is chosen using a shortest-path-based solution selection method. In comparison to previous two-stage methods, experimental results show significant runtime improvements and a reduction in the number of additional CNOT gates.

Although the reference work is a significant step forward in quantum layout synthesis, it is still limited to quantum hardware compilation. It discusses mapping efficiency and logical gate transformations, but it ignores power optimization, CMOS transistor-level implementation, and the traditional hardware realization of reversible logic. As a result, it does not offer a foundation for implementing reversible quantum gates in VLSI systems, despite lowering the overhead of logical gates for quantum processors. The necessity for an additional hardware-oriented strategy is driven by this constraint.

4. Proposed work

The proposed approach focuses on the classical VLSI realization of quantum logic primitives instead of mapping quantum hardware. The goal is to build synthesizable CMOS architectures that properly execute CNOT, Toffoli, and multi-controlled Toffoli operations while maintaining reversibility and minimizing hardware complexity, rather than maximizing qubit placement under coupling limitations.

A target signal is conditionally inverted by the Controlled-NOT gate in response to a control input. The XOR of the control signal and the initial target is how the target output is represented in Boolean form. A static CMOS XOR gate topology can be simply transferred to this functionality. Full voltage swing, balanced propagation latency, and less dynamic switching are all guaranteed by the optimized XOR implementation in the suggested architecture. Reversibility is naturally maintained by leaving the control signals at the output unaltered.



CMOS XOR Gate (CNOT Gate) CMOS Toffoli Gate (CCNOT Gate)

Fig 2: Transistor-Level CMOS Realization of CNOT and Toffoli Gates

By adding a second control input, the Toffoli gate expands on this function. The logical AND of two control inputs and the XOR of the target input can be used to define its Boolean function. A two-stage AND–XOR structure is used in the suggested architecture to provide this behaviour. An XOR stage that conditionally flips the target is driven by the intermediate signal that is produced after the control signals are initially merged using a low-fan-in AND gate. By using this structured decomposition, needless signal buffering is avoided and logic depth is reduced. The suggested mapping guarantees bijective transformation between input and output vectors, in contrast to irreversible methods that might recalculate intermediate signals or eliminate information.

The architecture is extended to multi-controlled Toffoli gates in order to allow for scalability. The combined control condition for a gate with n control inputs is calculated using a hierarchical AND-tree structure. The tree is set up to avoid excessive propagation latency by limiting fan-in and balancing delay at each stage. One XOR stage that is connected to the target input is driven by the final AND output. Verilog modules that are parameterized are used to define the design, enabling synthesis for arbitrary control widths without requiring structural changes.

The suggested work presents a reversible D flip-flop architecture in addition to combinational reversible logic. Reversibility is violated by conventional flip-flops, which by nature delete data during state transitions. Toffoli-based gating and regulated feedback are used in the proposed reversible D flip-flop to guarantee that state transitions are still logically invertible. Building larger reversible processors and fault-tolerant control circuits is made possible by this sequential extension.

AND–XOR CMOS Mapping

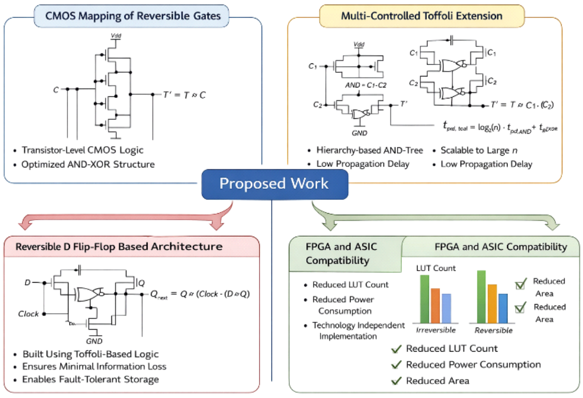
Multi-Control AND-Tree Delay Equation

Dynamic Power Equation

Reversible D Flip-Flop Equation

Synthesizable Verilog HDL is used to implement the entire architecture, and simulation is used for validation. While ASIC synthesis verifies viability using standard-cell libraries, FPGA synthesis shows compatibility with LUT-based mapping. Due mainly to controlled switching activity and structured AND–XOR mapping, area utilization and power consumption are lower than with traditional logic blocks implementing equivalent conditional functionality.

The proposed technique targets physical hardware realization as opposed to current quantum layout synthesis frameworks that reduce SWAP insertion and CNOT count at the logical abstraction level. It bridges the gap between traditional VLSI design and quantum logic theory by translating reversible quantum gate behaviour into effective CMOS circuits. The resulting architecture serves as a basis for safe hardware implementations, quantum-inspired accelerators, and low-power reversible computing systems.



- Transistor level CMOS Realization of CNOT and Toffoli gates overall architecture of the proposed reversible VLSI framework including CMOS mapping, multi-controlled extension, reversible sequential design, and FPGA/ASIC compatibility.

- The transistor-level implementation of reversible gates employing optimized AND-XOR CMOS architectures is shown in the first block. In this step, a two-stage AND–XOR cascade is used to actualize the Toffoli gate, while a static CMOS XOR network is used to achieve the basic CNOT operation. This mapping reduces the number of transistors and switching overhead while maintaining reversibility. This block allows synthesis in common digital design flows by explicitly translating reversible Boolean behavior into physical CMOS pull-up and pull-down networks, in contrast to abstract quantum gate representations.

The architecture is extended to multi-controlled Toffoli gates in the second block. The composite control condition is calculated using a hierarchy-based AND-tree structure rather than high fan-in logic. With regard to the amount of control inputs, this structured decomposition lowers the propagation delay growth from linear to logarithmic. A final XOR stage that conditionally updates the target line is then driven by the calculated control signal. Without causing undue routing congestion, this modular architecture enables adjustable scalability and effective mapping onto FPGA lookup tables or ASIC standard cells.

A reversible D flip-flop architecture built with Toffoli-based logic primitives is presented in the third block. Traditional sequential elements violate reversibility restrictions because they naturally lose information during state transitions. The suggested reversible flip-flop uses controlled XOR operations powered by clock and data inputs to selectively update the output state while maintaining logical bijectivity. Deterministic backward computing and fault-tolerant storage techniques, which are necessary for hardware accelerators inspired by quantum mechanics, are supported by this framework.

Compatibility with realistic implementation is the focus of the last subsystem. The suggested design can be immediately mapped onto FPGA devices using LUT-based synthesis or onto ASIC technologies utilizing standard-cell libraries because it is specified using synthesizable Verilog HDL. Compared to analogous irreversible implementations, the structured AND–XOR mapping improves area efficiency and lowers dynamic power consumption by reducing logic depth and switching activity. Furthermore, mobility across various fabrication nodes is guaranteed by the technology-independent design.

5. Results and Discussion

The designs are developed in Xilinx Vivado tool for the hardware of choice is 28nm CMOS technology based Artix-7 FPGA board (xc7z020clg484-1). The system requirements include windows 10 OS, 4 GB RAM installed with Xilinx Vivado 2023.2. The simulation result of existing and proposed designs are shown fig.4. (a) & (b).

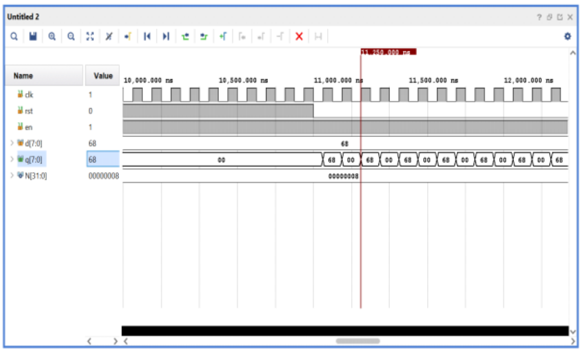


Fig 3:(a) Simulation Result of toffoli reversible quantum circuit

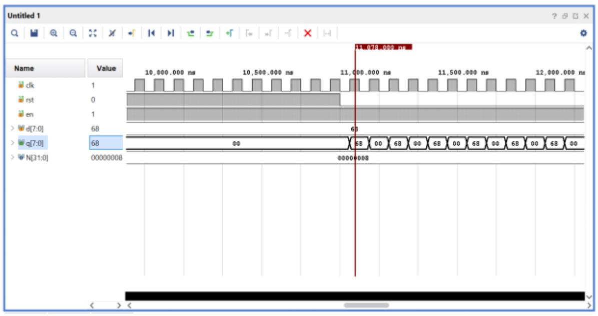


Fig 3:(b) Simulation Result of toffoli reversible quantum circuit with 4 controls

Verilog HDL was used to build the suggested VLSI implementation of CNOT and Toffoli-based reversible quantum circuits, which were then synthesized in Xilinx Vivado. The synthesis technology schematic confirms that the reversible quantum gates are implemented using XOR and AND–XOR based CMOS logic structures. The multi-controlled Toffoli circuit uses 28 cells, 19 input ports, and 39 nets because of extra control signals, whereas the CNOT reversible circuit uses about 27 cells, 8 input ports, and 37 nets.

LUTs, buffers, and flip-flops are used to construct the internal reversible control module, which has nine cells, six I/O ports, and fifteen nets. The findings show that the suggested design achieves effective hardware realization with minimal space overhead, which qualifies it for reversible VLSI designs and quantum circuit emulation.

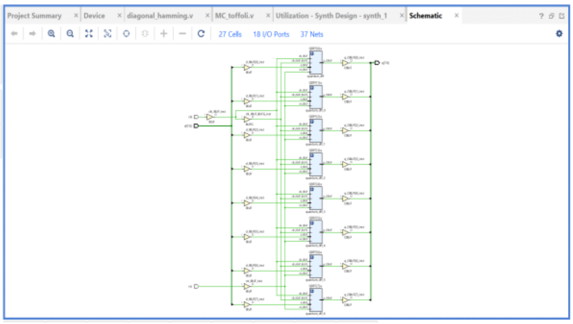


Fig 4:(a) Technology Schematic of Existing Design

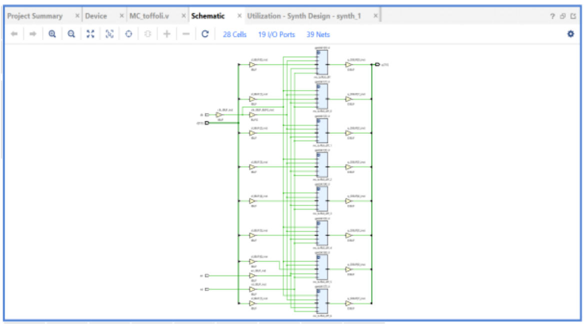


Fig4:(b) Technology Schematic of toffoli reversible quantum circuit

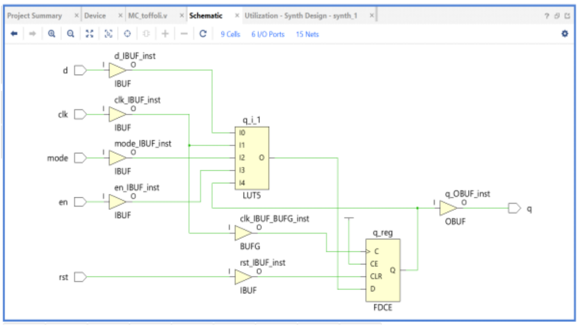


Fig 4:(c) Technology Schematic of toffoli reversible quantum circuit with 4 control signals

Parameter	Existing Design	MC Toffoli DFF	MC4 Toffoli DFF (Proposed)
Maximum Setup Delay	5.733	6.113	4.783 ns
Logic Delay	1.800	1.800	3.103 ns
Net Delay	3.933	4.313	1.680 ns
Minimum Hold Delay	1.354	1.354	0.384 ns
Total On-Chip Power	4.246	4.207	0.27 W
Dynamic Power	3.996 W	3.960	1.164
Static Power	1.250	1.247	1.107
Signal Power	1.119	1.121 W	0.020 W
Logic Power	1.41	1.41	0.009 W
I/O Power	3.836	3.789	0.135 W
Junction Temperature	74°C	73.5°C	28.1°C

Table.1: Comparison

When compared to the current and MC Toffoli designs, the comparison results demonstrate that the suggested MC4 Toffoli based reversible D flip-flop greatly increases power efficiency. The overall on-chip power is lowered from 4.246 W to 0.27 W, indicating a significant decrease in switching and I/O power. Better timing performance is also indicated by the maximum setup delay, which drops to 4.783 ns. These findings verify that the suggested architecture offers an effective low-power reversible logic implementation appropriate for VLSI systems with quantum inspiration.

6. Conclusion

In this paper, reversible quantum circuits based on CNOT and Toffoli were implemented in VLSI utilizing Verilog HDL and FPGA synthesis. Timing and power analyses were performed on the suggested multi-controlled Toffoli-based reversible D flip-flop. The findings demonstrate that the suggested design significantly reduces power consumption while preserving stable timing performance, making it appropriate for reversible computing and low-power quantum-inspiredapplications. Future research can concentrate on refining the architecture for ASIC-based quantum control and fault-tolerant quantum computing systems, as well as constructing larger reversible circuits like registers, counters, and arithmetic units.

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