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TWO STEP TIME TO DIGITAL CONVERTER

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Abstract - *Time-to-Digital Converters (TDCs) are widely used digital circuits for measuring very small-time intervals between signal events in high-precision systems. This project presents the design and implementation of a two-level TDC architecture that combines both coarse and fine time measurement techniques to achieve improved resolution and dynamic range. The coarse measurement is implemented using a counter-based TDC that counts clock cycles between start and stop signals, offering simplicity and a wide measurement range but limited resolution. To overcome this limitation, a fine measurement stage is introduced using a buffer delay line, which subdivides a single clock period into smaller intervals based on the known propagation delay of logic gates. The hybrid TDC combines these approaches to achieve improved resolution and an extended measurement range, making it suitable for applications such as time-of-flight measurements, digital communication systems, radar systems and precision instrumentation. However, the hybrid architecture results in higher power consumption due to increased switching activity. To address this issue, a flip-flop based clock gating technique is proposed as a power optimization extension. Simulation results demonstrate that the proposed clock gating approach significantly reduces power consumption while maintaining the functional performance of the system.*

Key Words: Time-to-Digital Converter (TDC), Counter-Based TDC, Buffer Delay Line TDC, Flip flop based clock gating, High-Resolution Timing Measurement.

1. INTRODUCTION

Time measurement plays an important role in many modern electronic systems such as time-of-flight sensors, radar systems, high-speed communication circuits, and scientific instrumentation. In these applications, the ability to measure very small time differences between digital events is essential for achieving high accuracy and reliable system performance. Time-to-Digital Converters (TDCs) are digital circuits specifically designed to convert a time interval between two signals into a digital representation [1].

Several architectural approaches have been developed to implement Time-to-Digital Converters with different trade-offs between resolution and hardware complexity. One commonly used approach is the counter-based TDC, where a digital counter measures the time interval by counting the number of clock cycles between the start and stop signals [3]. This architecture is simple and capable of measuring long time intervals; however, its resolution is limited by the period of the reference clock.

To obtain finer timing resolution, delay-line based TDC architectures are often used [2]. In this method, a chain of delay elements such as buffers or inverters creates small propagation delays that divide a clock period into multiple smaller intervals. By observing how far the signal propagates through the delay chain, it becomes possible to determine fine timing differences within a clock period. In this work, both techniques are combined to form a hybrid Time-to-Digital Converter architecture. The counter-based stage performs coarse time measurement while the buffer delay line stage provides fine time interpolation within a clock cycle. This combined approach improves the overall measurement accuracy while maintaining a wide dynamic range.

2. METHODOLOGY

Time-to-Digital Converters (TDCs) measure the time interval between two digital events and convert it into a corresponding digital value. These circuits are widely used in applications such as time-of-flight measurement systems, high-speed communication interfaces, and scientific instrumentation where accurate time interval measurement is required. TDC architectures are typically categorized into coarse measurement techniques and fine measurement techniques [1]. Coarse TDCs generally rely on clock-based counters to measure time intervals in terms of clock cycles, providing a large dynamic range but limited resolution. In contrast, fine TDC architectures utilize delay elements to measure small time differences within a clock period, enabling higher timing resolution.

2.1 Counter-Based TDC

The counter-based TDC is used to perform coarse time interval measurement between two digital events [3]. In this approach, a synchronous counter begins counting clock pulses when the start signal becomes active. The counter increments on every rising edge of the reference clock and continues counting until the stop signal is received. Once the stop signal occurs, the counter value is captured and stored as the coarse measurement result. The measured time interval is proportional to the number of counted clock cycles and the clock period.

The time interval can be calculated as:

$$T = N \times T_{clk}$$

$$T = (C_{stop} - C_{start}) \times T_{clk}$$

Here,

N = Number of clock cycles = $(C_{stop} - C_{start})$

T_{clk} = Clock period

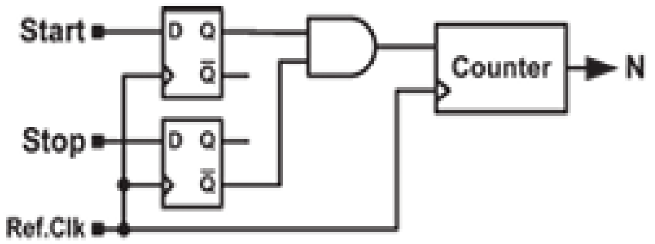


Fig.1: Counter based TDC

This architecture offers a wide measurement range and simple hardware implementation; however, its timing resolution is limited by the clock period.

The design is described using Verilog HDL and simulated using Vivado to verify the counting operation and timing behavior.

2.2 Buffer Delay Line TDC

To achieve finer time resolution, a buffer delay line based TDC is implemented. In this approach, a series of delay elements such as buffers or inverters are connected in sequence to form a delay chain [2]. Each stage introduces a small propagation delay. Once the start signal is applied, it begins traveling through a sequence of delay elements arranged in a chain.

When the stop signal is detected, the states of all delay stages are sampled at the same instant using flip-flops or registers. The captured outputs form a pattern known as a thermometer code, which indicates how far the signal has propagated through the delay line. The count of active stages (logic '1') is converted into its equivalent binary representation to obtain the fine measurement.

The fine time interval is determined as:

$$T_{fine} = N_{ones} \times T_{delay}$$

Here,

N_{ones} = Number of 1's in thermometer code

T_{delay} = Propagation delay of one buffer stage

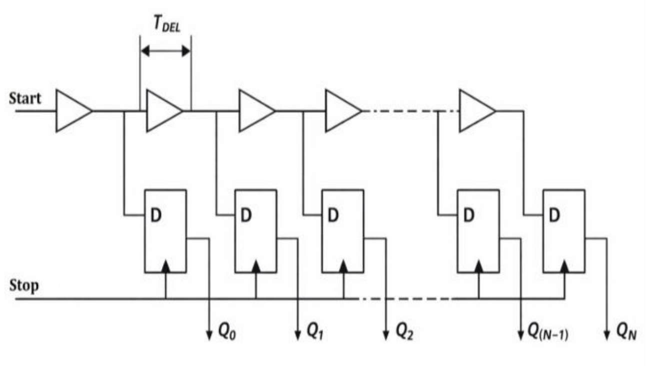


Fig.2: Buffer delay line TDC

The design is described using Verilog HDL and simulated using Vivado to verify the propagation behavior of the delay and generation of the thermometer code. This method provides high time resolution, typically in the picosecond or sub-nanosecond range.

2.3 Hybrid TDC

In the proposed design, both coarse and fine measurement techniques are combined to form a hybrid TDC architecture [4]. The coarse measurement stage determines the time interval by counting complete clock cycles between the start and stop events. At the same time, the delay line structure measures the fractional portion of the time interval within a single clock cycle.

During operation:

1. The counter begins counting clock cycles after the start signal is detected.
2. The delay chain monitors the signal progression within a single clock cycle to capture fine timing information.
3. At the moment the stop signal is received, both the counter output and delay-line states are recorded together.

The total measured time interval is obtained by combining the coarse and fine measurements as:

$$T_{total} = (C_{coarse} \times T_{clk}) + (C_{fine} \times T_{delay})$$

Here,

C_{coarse} = Number of clock cycles (N)

C_{fine} = Number of 1's in thermometer code (N_{ones})

T_{clk} = Clock period (e.g., 10ns = 10,000ps)

T_{delay} = Propagation delay of one buffer stage (e.g., 100ps)

This hybrid architecture improves measurement accuracy by combining the wide range of counter-based measurement with the high resolution of delay-line interpolation.

The entire design is implemented using Verilog HDL and simulated in the Vivado environment, where waveform analysis is used to verify the functionality of both measurement stages. The simulation results showing the coarse count, thermometer code, and fine count are presented in the results section.

2.4 Power Optimization Using Flip-Flop Based Clock Gating

Although hybrid TDC architectures provide improved measurement resolution, they may consume higher power due to continuous switching activity in the clock network and delay line circuitry. To address this issue, a flip-flop based clock gating technique is introduced.

In this approach, the system clock is controlled using a gating circuit consisting of an AND gate and a flip-flop based enable signal. The clock is allowed to propagate to the TDC circuitry only when the measurement process is active. When the system remains idle, the clock signal is disabled, preventing unnecessary switching activity.

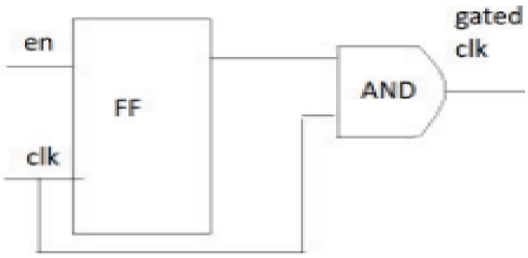


Fig.3: Block Diagram of Flip flop Based Clock gating

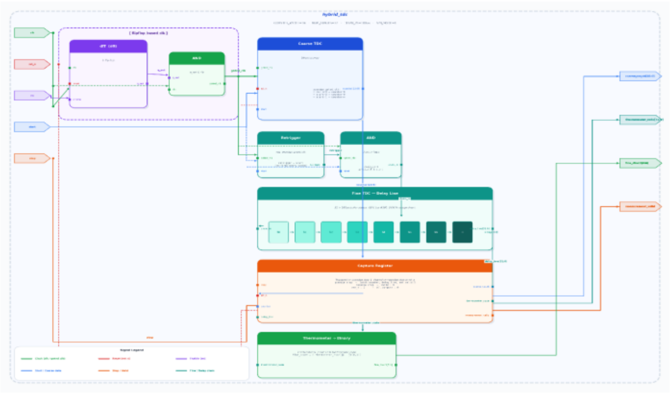


Fig.4: Proposed block diagram of Hybrid TDC with flip flop based clock gating

By reducing redundant clock transitions, the proposed clock gating mechanism significantly lowers dynamic power consumption while maintaining the functional behavior and timing characteristics of the TDC system.

3. RESULTS

The simulation waveforms, schematic and various parameters of TDC architecture are shown below.

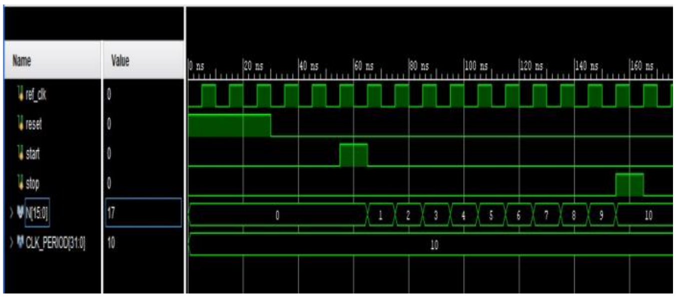


Fig.5: Simulation waveform of counter TDC

The waveform illustrates the working behavior of the counter-based TDC during coarse time measurement. The ref_clk signal provides the reference clock with a period of 10 ns. When the start signal becomes active, the counter begins incrementing on each rising edge of the clock. The counter value increases sequentially from 1 to 10 until the stop signal occurs. Since the counter records 10 clock cycles, the measured time interval is calculated as T = 10 × 10 ns = 100 ns. This confirms that the counter-based TDC correctly measures the time difference between the start and stop signals.

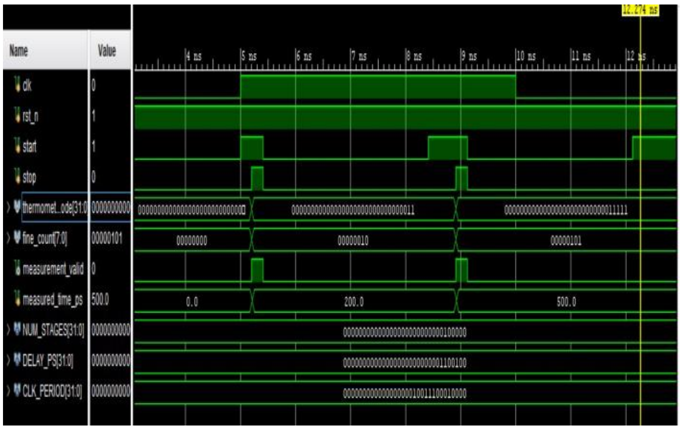


Fig.6: Simulation waveform of buffer delay line TDC

The waveform illustrates the fine time measurement using a buffer delay line. When the start signal is applied, the signal propagates through multiple delay stages, each introducing a delay of approximately 100 ps.

At the arrival of the stop signal, for example, the thermometer code shows five 1's producing a fine count of 5. Therefore, the measured fine time interval is 5 × 100 ps = 500 ps, confirming the correct operation of the delay-line based TDC

Fig.7: Simulation waveform of Hybrid TDC

The waveform illustrates the operation of the hybrid Time-to-Digital Converter that combines coarse counter measurement and fine delay-line interpolation. When the start signal becomes active, the coarse counter begins counting the clock cycles of the gated clock, while the delay line measures the fractional portion of the interval.

For example, the coarse counter records values such as 3, 7, 15, and 20 clock cycles, corresponding to 30 ns, 70 ns, 150 ns, and 200 ns respectively for a 10 ns clock period. The delay line simultaneously produces fine counts such as 5, 10, 15, and 18, representing 500 ps, 1000 ps, 1500 ps, and 1800 ps with a 100 ps delay per stage. The total measured time is obtained by combining the coarse and fine values, confirming correct hybrid TDC functionality.

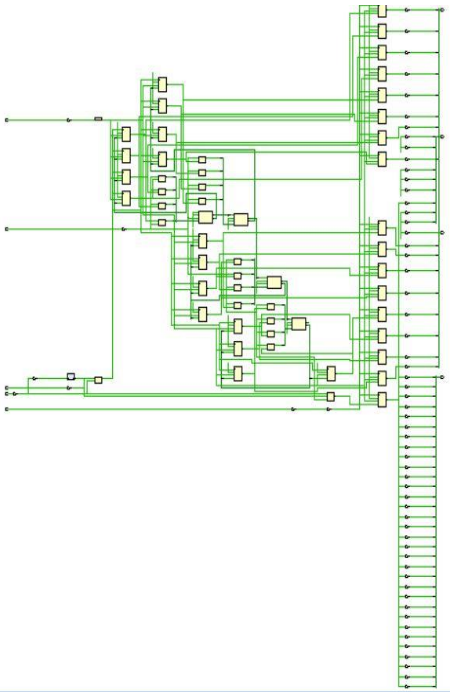
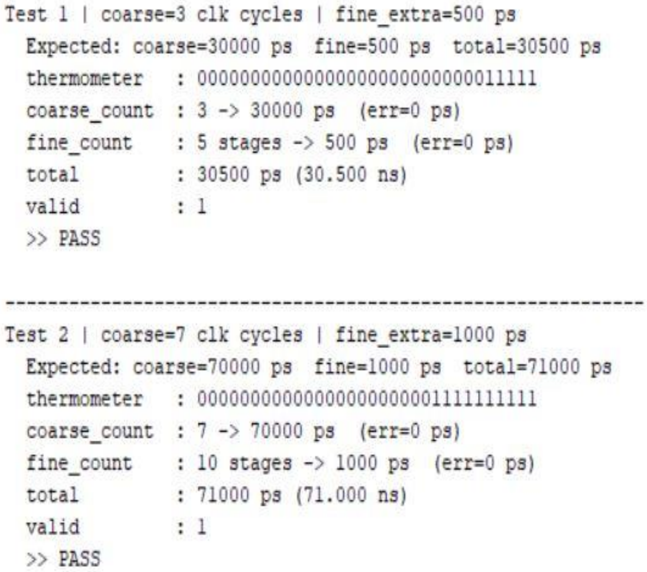


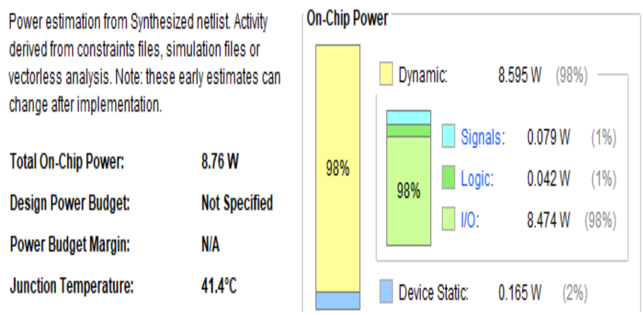
Fig.8: Test cases of Hybrid TDC



```
Test 1 | coarse=3 clk cycles | fine_extra=500 ps
  Expected: coarse=30000 ps  fine=500 ps  total=30500 ps
  thermometer   : 00000000000000000000000000011111
  coarse_count  : 3 -> 30000 ps  (err=0 ps)
  fine_count    : 5 stages -> 500 ps  (err=0 ps)
  total         : 30500 ps (30.500 ns)
  valid         : 1
  >> PASS

------------------------------------------------------------
Test 2 | coarse=7 clk cycles | fine_extra=1000 ps
  Expected: coarse=70000 ps  fine=1000 ps  total=71000 ps
  thermometer   : 00000000000000000000001111111111
  coarse_count  : 7 -> 70000 ps  (err=0 ps)
  fine_count    : 10 stages -> 1000 ps  (err=0 ps)
  total         : 71000 ps (71.000 ns)
  valid         : 1
  >> PASS
```

Fig.9: Schematic of Hybrid TDC

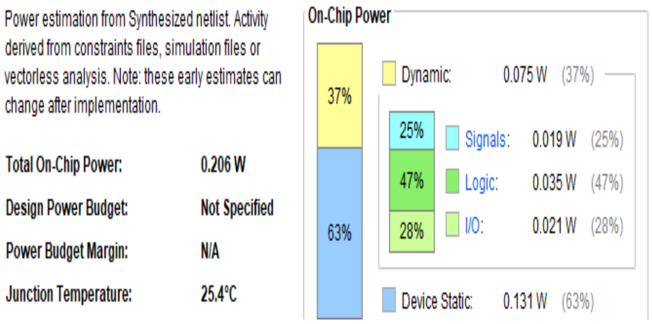


Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 8.76 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 41.4°C

On-Chip Power
Dynamic: 8.595 W (98%)
Signals: 0.079 W (1%)
Logic: 0.042 W (1%)
I/O: 8.474 W (98%)
Device Static: 0.165 W (2%)

Fig.10: Power of Hybrid TDC

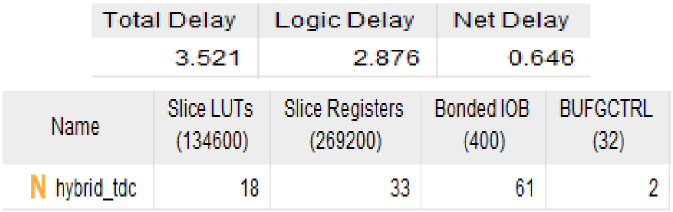


Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.206 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 25.4°C

On-Chip Power
Dynamic: 0.075 W (37%)
Signals: 0.019 W (25%)
Logic: 0.035 W (47%)
I/O: 0.021 W (28%)
Device Static: 0.131 W (63%)

Fig.11: Area and delay of Hybrid TDC



Total Delay	Logic Delay	Net Delay
3.521	2.876	0.646

Name	Slice LUTs (134600)	Slice Registers (269200)	Bonded IOB (400)	BUFGCTRL (32)
N hybrid_tdc	18	33	61	2

Fig.12: Power of Hybrid TDC with flip flop based clock gating

The synthesis results clearly indicate that the implemented clock gating technique significantly improves power efficiency. Before optimization, the synthesized design consumed a total on-chip power of 8.76 W, where the dynamic power contributed 8.595 W (98%) and the static power was 0.165 W (2%). After applying the flip-flop based clock gating technique, the total on-chip power significantly decreased to 0.206 W. In the optimized design, the dynamic power reduced to 0.075 W, while the static power became 0.131 W. This reduction occurs because the clock is enabled only during active measurement periods, preventing unnecessary switching in idle conditions.

Overall, the proposed optimization reduces the total power from 8.76 W to 0.206 W, which corresponds to approximately 97.6% reduction in power consumption while maintaining the same functional operation and timing performance of the hybrid TDC system.

Table 1: Comparison of parameter values

Parameter	Hybrid TDC	Optimized Clock gated
Area [LUT's]	18	19
Power [W]	8.76	0.206
Static Power [W]	0.165	0.131
Dynamic Power [W]	8.595	0.075
Delay [ns]	3.521	3.521

4. CONCLUSION

In this work, a hybrid Time-to-Digital Converter (TDC) architecture has been designed and implemented by combining a counter-based coarse measurement stage with a buffer delay line based fine measurement stage. The coarse measurement stage determines the time interval by counting the clock cycles between the start and stop events, which allows the system to measure large time intervals. However, the timing resolution of this method is limited by the clock period. To improve resolution, a delay-line structure is utilized to capture fine timing variations within a single clock cycle.

By combining both approaches, the hybrid architecture provides improved timing resolution while maintaining a wide measurement range. The proposed design was implemented using Verilog HDL and simulated using the Vivado design environment. Simulation results verified the correct operation of the coarse counter, delay-line stages, and hybrid measurement mechanism.

Although the hybrid architecture improves measurement accuracy, it increases switching activity in the clock network, which results in higher power consumption. To address this issue, a flip-flop based clock gating technique was incorporated into the design. The clock gating mechanism enables the clock only during active measurement periods and disables it when the circuit is idle. As a result, unnecessary switching activity is reduced and dynamic power consumption is significantly lowered.

Experimental results show that the proposed optimization reduces power consumption from approximately 8.76 W to 0.206 W without affecting the functional performance or timing characteristics of the system. Therefore, the proposed hybrid TDC with clock gating provides an efficient solution for high-resolution and low-power time interval measurement applications.

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