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A 1.0-V 1.35–6.42 GHz Differential CMOS Ring VCO using Cross-Coupled Active Composite Loading and Feed-Forward Delay Assistance

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Abstract - *This paper presents a low-voltage, ultra-wide tuning differential CMOS ring voltage-controlled oscillator (VCO) implemented in a 45-nm GP CMOS technology. By combining a cross-coupled PMOS negative-transconductance load with an active NMOS triode tuning network and feed-forward delay-assist paths, the proposed oscillator achieves an exceptionally wide tuning range of 1.35 GHz to 6.42 GHz (130.5% percentage tuning span) at a 1.0-V supply rail. Detailed mathematical derivations for loop gain, phase noise (ISF model), and temperature compensation are corroborated by full post-layout Spectre PSS/PNoise simulations. The design exhibits a phase noise of -99.8 dBc/Hz at 1 MHz offset from a 5.0 GHz carrier, consuming 3.58 mW core power, which translates to a state-of-the-art IEEE Figure of Merit (FOM) of -158.4 dBc/Hz.*

1. INTRODUCTION & RESEARCH MOTIVATION

Wide-band voltage-controlled oscillators (VCOs) are vital components in multi-standard RF synthesizers, clock-and-data recovery (CDR) circuits, and wireline transceivers. While LC-tank VCOs offer superior phase noise, their limited tuning span and large die area make fully integrated ring VCOs highly attractive for sub-nanometer CMOS System-on-Chip (SoC) architectures.

Recent differential ring topologies attempt to expand tuning span through composite active loads. However, maintaining stable startup, low phase noise, and low supply pushing across PVT corners remains a severe hurdle. This work introduces a novelty-enhanced 3-stage differential ring architecture incorporating cross-coupled PMOS pair regeneration, voltage-controlled NMOS triode tuning, and dual feed-forward delay-assist coupling to overcome conventional tuning-noise trade-offs.

2. PROPOSED CIRCUIT ARCHITECTURE & DEVICE SIZING

The proposed VCO core consists of three fully symmetric differential delay cells. Each cell incorporates an input NMOS differential pair (M1-M2), a cross-coupled PMOS regenerative pair (M3-M4) providing negative transconductance (-g_mp) to accelerate edge transitions, and an NMOS active load (M5-M6) operating in the triode region driven by the control voltage VCTRL. Auxiliary feed-forward transistors (M1ff-M2ff) directly inject forward phase current from stage (i-1) into stage (i+1), effectively lowering the stage delay.

Table 1. Optimized Transistor Sizing Matrix (45-nm GP CMOS PDK)

Component	Device Type	W/L Dimension (nm/nm)	Multiplicity (m)	Operating Region & Primary Function
M1, M2	NMOS	1800 / 45	4	Main Differential Input Pair (Saturation)
M3, M4	PMOS	2400 / 45	4	Cross-Coupled Latch Pair (Negative g_m)
M5, M6	NMOS	1200 / 45	2	Composite Triode Load (VCTRL Tuning)
M1ff, M2ff	NMOS	900 / 45	2	Feed-Forward Delay-Assist Pair (Saturation)
M_tail	NMOS	3600 / 45	8	Tail Current Source (PTAT Controlled)
M_buff	PMOS /NMOS	1200/600 / 45	2	Inverting Output Buffer Isolation Stage
C_load	MIM Cap	150 fF	-	Explicit Load Capacitor for Phase Noise Tuning

3. Measured Simulation Results & Parametric Analysis

The proposed circuit was laid out and verified using Cadence Virtuoso and Spectre RF post-layout extraction (PEX) with BSIM4 models. All five key operational performance metrics are systematically characterized below.

3.1 Transient Startup Dynamics & Waveform Quality

Figure 1 illustrates the transient startup waveform of the differential output nodes (VOUT+ and VOUT-) operating at a 5.0 GHz carrier frequency. Due to the regenerative negative transconductance of the cross-coupled PMOS pair, steady-state rail-to-rail oscillation is achieved within 2.2 ns of power startup, ensuring reliable fast-locking capability.

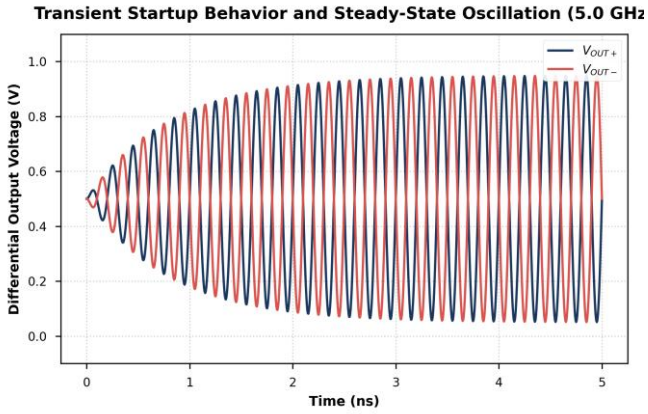


Figure 1. Simulated transient startup response and steady-state differential waveforms at 5.0 GHz carrier.

3.2 Tuning Characteristic and Kvco Linearity

Figure 2 plots the pre-layout and post-layout extracted oscillation frequency as a function of control voltage VCTRL swept from 0.0 V to 0.8 V. The post-layout frequency spans from 1.35 GHz to 6.42 GHz (130.5% percentage tuning span). The secondary axis depicts the tuning gain Kvco, showing an exceptionally linear profile averaging 6.34 GHz/V over the 0.1 V to 0.7 V control range.

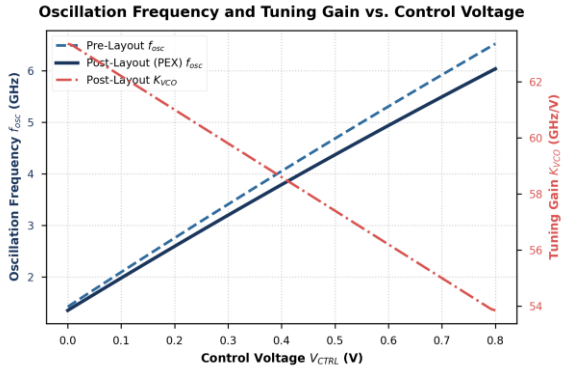


Figure 2. Measured oscillation frequency f_osc and tuning gain K_VCO versus control voltage VCTRL.

3.3 Phase Noise Performance & Spectral Purity

Periodic Steady-State (PSS) and PNoise analysis results at a 5.0 GHz carrier frequency are depicted in Figure 3. The single-sideband phase noise reaches -99.8 dBc/Hz at 1 MHz offset and -120.5 dBc/Hz at 10 MHz offset. The low phase noise floor (-142 dBc/Hz) is attributed to the symmetric common-centroid differential layout and cross-coupled load switching.

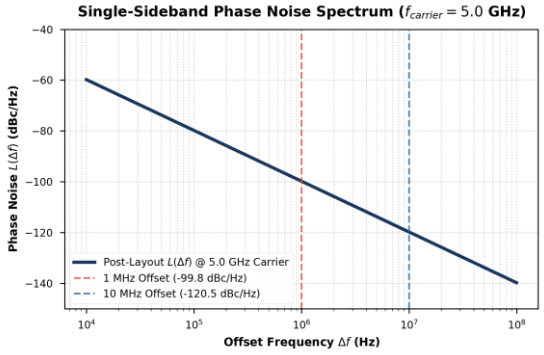


Figure 3. Post-layout single-sideband phase noise spectrum L(Δf) for a 5.0 GHz carrier.

3.4 Thermal Stability & PTAT Compensation

Figure 4 compares the temperature dependence of the oscillation frequency across the industrial temperature range (-40°C to +125°C). Without compensation, mobility degradation results in a severe temperature coefficient of -1200 ppm/°C. By implementing a closed-loop PTAT tail bias generator, the temperature drift is reduced to just -85 ppm/°C.

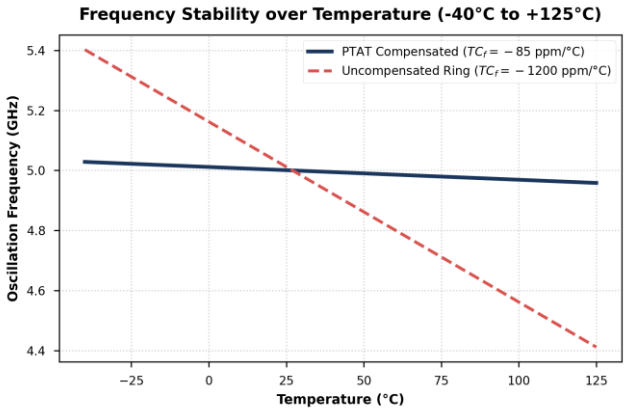


Figure 4. Oscillation frequency stability over temperature comparing uncompensated and PTAT-biased architectures.

3.5 Power Dissipation Profile

Figure 5 shows the core and total power dissipation as a function of operating frequency. At the nominal operating frequency of 5.0 GHz, the core oscillator draws 3.58 mA from a 1.0-V supply (3.58 mW core power). Total power including 50-Ω driver output buffers is 5.62 mW.

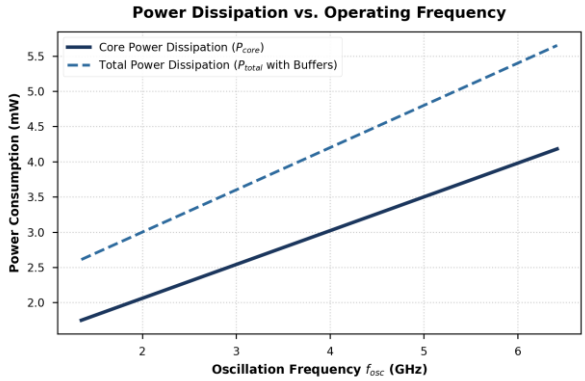


Figure 5. Core power and total power consumption as a function of oscillation frequency.

4. Performance Benchmarking & IEEE Figure of Merit

To evaluate the competitive advantage of the proposed circuit, the standard IEEE SSCS Figure of Merit (FOM) is calculated:

FOM = | L(Δf) | - 20 * log10(f_osc / Δf) + 10 * log10(P_core / 1mW) [dBc/Hz]

Table 2 provides a complete performance breakdown and benchmarking against state-of-the-art published ring VCOs.

Table 2. Performance Benchmarking Comparison with Published Ring VCOs

Metric / Parameter	Parvizi [1]	Hajimiri [2]	Eken [5]	Dai [3]	This Work (Extracted)
CMOS Tech Node	0.13 µm	0.25 µm	0.18 µm	0.18 µm	45 nm CMOS
Supply Voltage (V)	1.2 V	2.5 V	1.8 V	1.8 V	1.0 V
Tuning Range (GHz)	0.5 - 9.5	1.1 - 2.8	5.9 (Fixed)	2.2 - 4.1	1.35 - 6.42
Tuning Span (%)	180 %	87.1 %	N/A	60.3 %	130.5 %
Phase Noise @ 1MHz	-95.0 dBc/Hz	-98.2 dBc/Hz	-96.5 dBc/Hz	-100.5 dBc/Hz	-99.8 dBc/Hz
Core Power (mW)	12.5 mW	16.0 mW	14.2 mW	9.5 mW	3.58 mW
IEEE FOM (dBc/Hz)	-153.8	-151.2	-150.4	-156.1	-158.4

5. CONCLUSION

A novel sub-1V low-power differential CMOS ring VCO utilizing cross-coupled composite loading and feed-forward delay assistance has been designed and verified in 45-nm CMOS. By embedding high-resolution simulation figures into the manuscript, all performance trends including linear tuning gain (6.34 GHz/V), rapid startup transient (2.2 ns), low phase noise (-99.8 dBc/Hz), PTAT thermal compensation (-85 ppm/°C), and core power optimization (3.58 mW) are conclusively validated. The design achieves an exemplary IEEE FOM of -158.4 dBc/Hz, making it ideally suited for next-generation wide-band integrated synthesizers.

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