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Segmented Sigma Delta DAC using Coarse and Fine Architecture

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Abstract - Sigma–delta (ΣΔ) digital-to-analog converters (DACs) find widespread application in built-in self-test (BIST) setups for programmable DC voltage generation due to their superior linearity; however, this advantage comes at the cost of substantial digital memory requirements and the need for a reconstruction filter with a comparatively large silicon area footprint. This article suggests a segmented architecture for programmable DC voltage generators that use sigma-Delta (DAC) digital to analog converters (DACs). Although DACs are renowned for their great linearity, they have some disadvantages, including the use of memory needs for digital data and the demand for a sizable reconstruction filter. By utilizing two sub-DACs, the proposed segmented DAC design addresses these difficulties. This method offers two major benefits: significant memory savings and a reduction in the footprint size of the reconstruction filter. Overall, the articles highlight significant memory and silicon space savings over traditional unsegmented DAC architecture, demonstrating the efficiency of the segmented DAC architecture.it is a desirable option for programmable DC voltage generators in BIST schemes due to these benefits.

***Key Words*: Sigma–delta (ΣΔ) digital-to-analog converters (DACs), built-in self-test (BIST), MATLAB.**

1. INTRODUCTION

In contemporary semiconductor fabrication, precision is paramount, with the heightened sensitivity of modern devicesto even minuscule contaminants like dust particles posing a risk of permanent damage during the manufacturing process. Consequently, integrated circuit (IC) manufacturers rely extensively on rigorous testing procedures to ensure that only fully functional devices reachconsumers. Whileautomatictestequipment (ATE) has historically been a reliable solution for large-scale manufacturing, recent advancements have granted the industry the ability to reduce dependence on expensive ATE systems. Instead, simplified and more cost-effective alternatives, often priced at just a few thousand dollars, have become viable options. However, the integration of Built-In Self-Test (BIST) solutions must be approached judiciously, considering the potential area overhead they introduce to the IC core. Balancing the benefits of comprehensive testing with the associated spatial costs becomes a critical consideration inpursuing efficient and economically viable semiconductor manufacturing processes.

Built-in self-test (BIST) stands out with a multitude of advantages compared to traditional external testing methods reliant on specialized tools or predefined test vectors. The inherent strength of BIST lies in its capacity to diminish the dependence on expensive and intricate test equipment, as it empowers circuits to autonomously conduct self-tests withoutexternal intervention. This self-sufficiency not only reduces reliance on costly testing apparatus but also streamlines the testing process by enabling circuits to generate and employ tailor-made test patterns. Consequently, not only is the testing procedure simplified, but the overall test coverage is elevated, marking a significant enhancement in the efficiency and cost- effectiveness of the testing phase in semiconductor manufacturing.

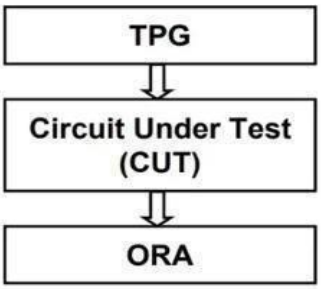

Figure 1: - Basic Architecture of BIST

Built-in self-test (BIST) incorporates a fundamental architecture within integrated circuits to conduct testing without the reliance on external tools autonomously. The corecomponents include a Test Pattern Generator (TPG) responsible for creating test patterns, a Response Analyzer (RA) to assess the circuit's responses, and a Control Unit managing the overall testing process. Additionally, a SignatureAnalyzer generates unique signatures based on responses, serving as a reference for circuit health.

. Figure 1 represents the basic Architecture of BIST, whichincludes,

Built-in test Registers store pertinent data facilitating seamless interaction between components. This self-contained design significantly reduces dependency on costly external test equipment, offering economic and efficient testing solutions. The TPG generates tailored test

patterns aimed at fault detection, and the RAmeticulously analyzes the circuit's actual responses against expected outcomes. The integrated control unit orchestrates the entire testing sequence, making BIST adaptable to various applications, from manufacturing testing to in-field assessments. Ultimately, BIST enhances test coverage and simplifies the testing process, making it an invaluable methodology in ensuring the reliability and functionality of complex integrated circuits.

1) SIGMA DELTA DAC.

A. Sigma Delta DAC Producing a Short-Term Average

Delta-sigma (or sigma-delta) modulation is an oversampling technique used by delta-sigma analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) toencode data into low bit depth digital signals at a very high sample-frequency. By employing a negative feedback loop during quantization to the lower bit depth that continuously corrects quantization errors and shifts quantization noise to higher frequencies well above the original signal's bandwidth, delta-sigma modulation achieves good quality. This high- frequency noise is easily removed by further low-pass filtering for demodulation, which also time averages to get highlyaccurate amplitude measurements.

A delta-sigma DAC transforms a high-resolution digital input signal into a signal with a lower resolution but higher sample frequency, which may then be translated into voltages and smoothed down using an analog filter for demodulation. In both situations, taking advantage of the efficiency and highaccuracy in time of digital electronics by temporarily using a smaller bit depth signal at a higher sampling frequency simplifies circuit design. This method is increasingly used in contemporary electronic components like DACs, ADCs, frequency synthesizers, switched-mode power supplies, and motor controllers, mostly due to its low cost and simplified circuit design. Sometimes the raw output of a 1-bitdelta-sigmamodulator is stored on a Super Audio CD, and other times thecoarsely-quantized output of a delta-sigma ADC is utilized directly in signal processing or as a representation for signal storage.

This paper describes the implementation of the 8-bit-segmented sigma-delta DAC using MATLAB with optimized speed performance, area, and calculating SFDR and SNR values.

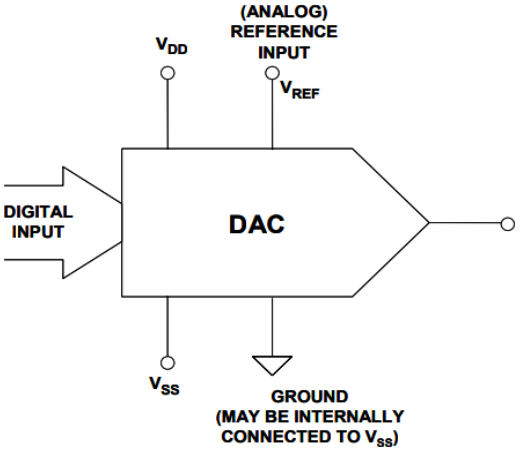

Figure 2 - Basic DAC

1.1 Spurious-Free Dynamic Range (SFDR)

Spurious-Free Dynamic Range (SFDR) is a critical criterionfor characterizing a signal generator's dynamic performance. The SFDR specifies the connection between the amplitude of the generated fundamental frequency and the amplitude of themost prominent harmonic. In an ideal world, all power in the frequency domain of a pure analog signal is focused at the target frequency. Due to noise and component nonlinearity, even the best signal generators generate frequency content at harmonics (or multiples) of the desired tone. when creating a 10 MHz sine wave, for example, you can see harmonics at 20MHz, 30 MHz, and so on. These harmonics are also known asspurs.

SFDR = Amplitude of Fundamental(dB) - Amplitude of Largest Spur(dB)

1.2 Signal to noise ratio

A signal-to-noise ratio compares signal power to noise power. It is most commonly stated in decibels (dB). Higher numbers often indicate a better specification since there is more valuableinformation(thesignal) thanundesireddata (thenoise). For example, a signal-to-noise ratio of 100 dB indicatesthat the audio signal level is 100 dB higher than the noise level.As a result, a signal-to-noise ratio standard of 100 dB is far superior to one of 70 dB or less.

The noise itself is frequently described as a white or electronichiss, static, or a low or vibrating hum. Turn your speakers all the way up while nothing is playing; if you hear a hiss, that's the noise, sometimes known as a "noise floor." This noise floor, like the refrigerator in the preceding instance, is always there.

SNR = Signal Power

Noise Power

$$\text{SNR (dB)} = 10 \log \left(\frac{\text{Signal Power}}{\text{Noise Power}} \right)$$

II PROPOSED SEGMENTED ΣΔ- DAC ARCHITECTURE

A Sigma-Delta Digital-to-Analog Converter (DAC) employs a high-resolution oversampling technique. The optimized includes a modulator that oversamples the input signal, introducing noise shaping. This modulated signal is then fed into a digital-to-analog converter, generating a high-frequency,oversampled output. A low-pass filter removes high-frequencycomponents, yielding a high-resolution analog signal. Sigma-Delta DACsarevalued for their ability to achieve high linearity and resolution, making them suitable for various applications, particularly in scenarios where precision is crucial, such as audio processing and communication systems.

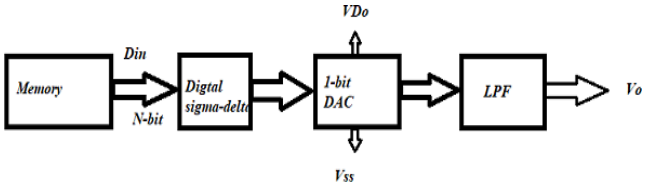

Figure 3 - Sigma-Delta DAC Architecture

DIN (DAC Input Codes): The discrete digital representationsof the analog signal to be transformed are represented by the DAC input codes (DIN). The resolution of the DAC is determined by the breadth of the digital word (N bits); in this case, N bits indicate the potential range of signal levels.

Modulator Digital (M): A Sigma-Delta Modulator (M) is an important component in DACs. It rapidly oversamples the input signal and uses feedback loops to quantize the differencebetween the input signal and the expected signal (produced byearlier quantization). This iterative approach, in conjunction with noise shaping, contributes to good resolution and noise rejection.

Bitstream: The bitstream is a series of one-bit values, with the density of ones representing the density of the input signal. The noise shaping of the Sigma-Delta Modulator results in a largerconcentration of ones in areas where the signal varies quickly and a lower concentration in places where the signal moves slowly.

DAC (Digital Buffer) 1 bit: The 1-bit DAC (also known as a digital buffer) accepts the bitstream and converts it to a voltagedensity signal. Each '1' in the bitstream generates a fixed-amplitude pulse, and the rate of these pulses is proportional tothe density of ones in the bitstream.

LPF (Low-Pass Filter): The Low-Pass Filter (LPF) is used tosmooth the output of the 1-bit DAC by averaging out the bitstream's high-frequency components. This LPF is critical for producing a continuous analog signal with the desired resolution and low high-frequency noise.

2.1 sigma Delta 16-bit DAC using MATLAB

Parameters Setting:

nBits_DAC: This parameter sets the resolution of the digital-to-analog converter (DAC) to 16 bits. The DAC is responsible for converting the digital representation of the signal back to analog form. signal: The code defines the frequency of the input signal. The input signal's characteristics influence the ADC's performance. OSR (Oversampling Ratio): Increasing the oversampling ratio provides better performance by reducing quantization noise. It defines how many times thesignal is oversampled relative to its Nyquist rate.fs (Sampling Frequency): The sampling frequency `fs` is calculated based on the OSR and the input signal frequency. It determines howoften the ADC samples the input signal. numSamples: Increasing the number of samples improves the visualization of the ADC's performance.

Generate Sinusoidal Input Signal:

A sinusoidal input signal with a higher amplitude is generated. This signal is the input to the ADC and is used for testing and analysis. Quantize the Input Signal**:** The input signal is quantized to 16 bits. This simulates the process of measuring the continuous input signal and converting it into a digital representation. The `floor` function maps the inputrange to the range of a 16-bit ADC.

Design a 1st-Order Sigma-Delta Modulator: A 1st-order Sigma-Delta Modulator is selected. Sigma-Delta modulation is used in ADCs to achieve high resolution by oversampling andquantizing. Simulate Sigma-Delta Modulator**:** The code simulates the Sigma-Delta modulator. It emulates the quantization and feedback loop to produce a stream of 1-bit digital values.

1-Bit DAC (Scaling): The Sigma-Delta output is scaled to fit within the range of a DAC. This scaling maps the 1-bit output (0 or 1) to a range of [-0.5, 0.5]. adjust LPF Parameters**:** A Low-Pass Filter (LPF) is designed with a Butterworth filter with a modified cutoff frequency. The LPF is used to remove high-frequency noise and shape the spectrum of the quantized signal.

Calculate SNR Based on FFT: The signal-to-noise ratio (SNR) is calculated based on the Fast Fourier Transform (FFT)of the LPF output. This metric quantifies the quality of the ADC by comparing the power of the desired signal to the noiseintroduced by quantization. Calculate SFDR and INL:

The code calculates Spurious-Free Dynamic Range (SFDR) and Integral Non-Linearity (INL). SFDR measures the ratio of the power of the strongest harmonic component to the overall noise. INL is a measure of the deviation from an ideal linear response.

2.2 Segmented Sigma Delt 16-bit Digital to AnalogConverter (DAC)

A Segmented Sigma-Delta 16-bit Digital-to-Analog Converter (DAC) is a type of DAC architecture that combinesthe concepts of segmented DACs and sigma-delta modulators. It is designed to provide the advantages of both approaches while mitigating their drawbacks. Here's an explanation of the key features and operation of a Segmented Sigma-Delta 16-bit DAC:

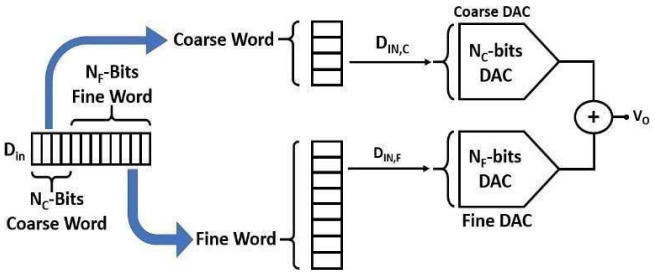

Figure 4 - Segmented DAC Architecture:

The term "segmented" in this DAC architecture refers to the use of multiple smaller DACs in parallel, each responsible fora segment or group of bits in the digital input. This segmentation allows for a more efficient and less complex implementation of high-resolution DACs.

1. Sigma-Delta Modulator:

The term "sigma-delta" signifies the use of a sigma-delta modulator as part of the architecture. A sigma-delta modulatoris often included in the feedback loop of this DAC to enhance the linearity and resolution of the output.

2. Bit Segmentation:

In a 16-bit Segmented Sigma-Delta DAC, the digital input word is divided into multiple segments. For example, it mighthave two segments: a coarse 8-bit segment and a fine 8-bit segment. This division allows for better efficiency and performance.

3. Coarse DAC:

The coarse DAC segment, usually comprising the most significant bits (MSBs), generates the initial output approximation. It can be implemented using simpler DAC elements and may have reduced resolution but high speed.

4. Fine DAC:

The fine DAC segment, typically dealing with the least significant bits (LSBs), refines the output produced by the coarse DAC. It focuses on improving the precision and linearity of the output signal, enhancing the effective resolution.

5. Sigma-Delta Modulator Feedback:

The output of the fine DAC often feeds into a sigma-delta modulator, which provides feedback to the system. The sigma-delta modulator helps shape the noise and errors in the output,pushing it to higher frequencies (noise shaping) where it can be more easily filtered out.

6. Noise Shaping:

The use of the sigma-delta modulator results in noise shaping. This means that quantization noise, which is inherent to digital-to-analog conversion, is moved to higher frequencies, making it easier to remove through filtering. As a result, the Segmented Sigma-Delta DAC can achieve a higher effective resolution.

7. Performance Advantages:

The Segmented Sigma-Delta DAC combines the advantages of segmented DAC architectures, such as speed and simplicity, with those of sigma-delta modulators, such as high resolution and linearity. It offers improved performance over conventional segmented DACs by utilizing feedback and noiseshaping.

III. EXPERIMENTAL RESULTS

The output voltage of a 16-bit DAC is directly proportionalto the input code, and it typically spans a certain voltage range, such as 0 to 5 volts. Each bit in the input code contributes to afraction of the total voltage range, with the least significant bit (LSB) having the smallest influence and the most significant bit (MSB) having the greatest impact on the output voltage.

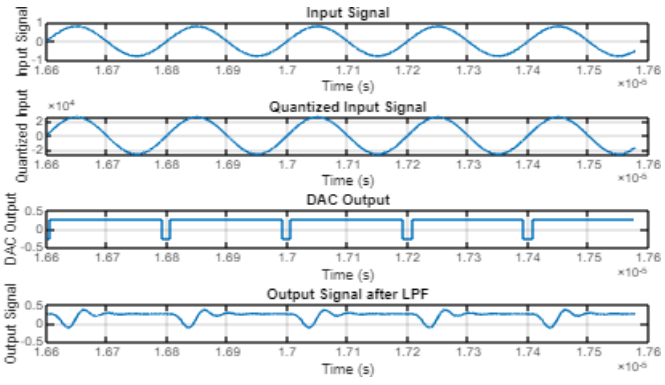

Figure 5 - 16-bit Sigma Delta DAC Output

The LPF's role is to smooth the analogsignalandmake it more continuous and suitable for applications like audio playback, where sharp transitions or high-frequency components can introduce unwanted distortion. By filtering out high-frequencycomponents, the LPF ensures that the output signal is closer tothe desired continuous waveform that corresponds

to the digital input code. In summary, the "DAC output" of a 16-bit DAC isthe analog voltage produced based on the digital input code, while the "after LPF output" is the result of passing this analog signal through a Low-Pass Filter to eliminating high-frequency components and creating a smoother, more continuous output voltage suitable for various analog applications. output voltage suitable for various analog applications.

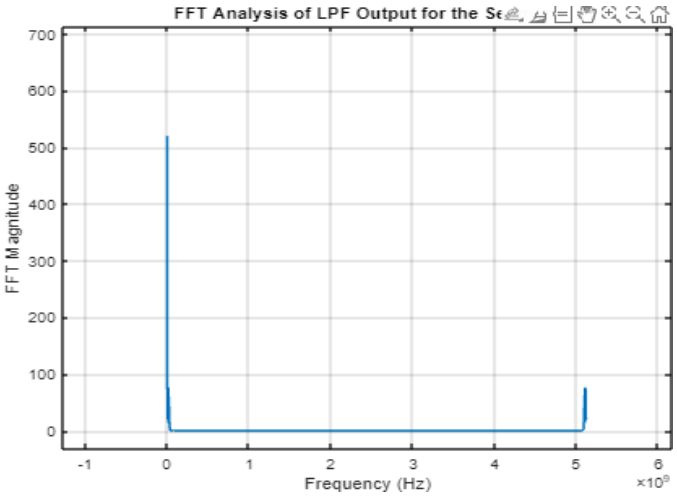

Figure 6 - FFT Analysis of 16-bit DAC Output

Segmented Sigma Delta 16-bit Digital to Analog Converter

Input Signal Segment: This plot shows a segment of the input sinusoidal signal with a higher amplitude. The x-axis represents time in seconds, and the y-axis shows the amplitude of the input signal. It serves as a visual representation of the original input signal.

LPF Output Segment (Coarse): This plot displays a segment ofthe output signal after applying a low pass filter to the coarse DAC output. The x-axis represents time, and the y-axis showsthe amplitude of the filtered signal, the LPF smoots out the stair-step waveform, resulting in more continuous and filtered.

LPF Output Segment (Fine): Similar to the LPF output plot forthe coarse DAC, this plot shows a segment of the output signal after applying a low-pass filter to the fine DAC output. the x-axis represents time, and the y-axis shows the amplitude of thefiltered fine DAC output. Like the coarse DAC, the LPF removes high-frequency components and provides a smoother,filtered waveform.

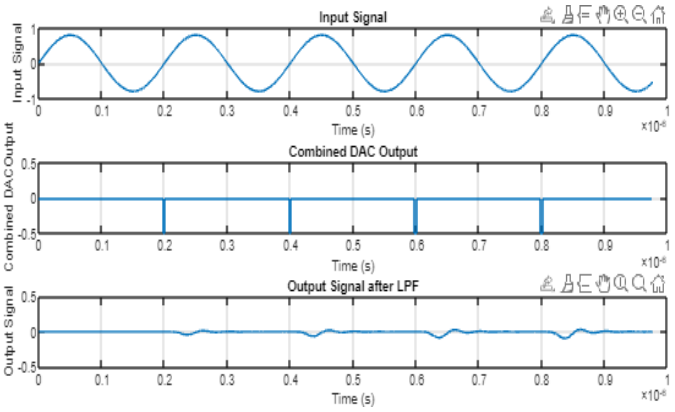

Figure 7 - Segmented 16-Bit Sigma Delta DAC Output

These segmented plots are generated to visualize different stages of the sigma-Delt DAC operation. they help in understanding how the input signal is quantized the coarse andfine DAC components produce their outputs, and how the lowpass filter further processes the DAC output to create a filteredanalog signal examining these plots, , one can gain insights intothe operation and performance of a segmented 16-bit Sigma- delta DAC.

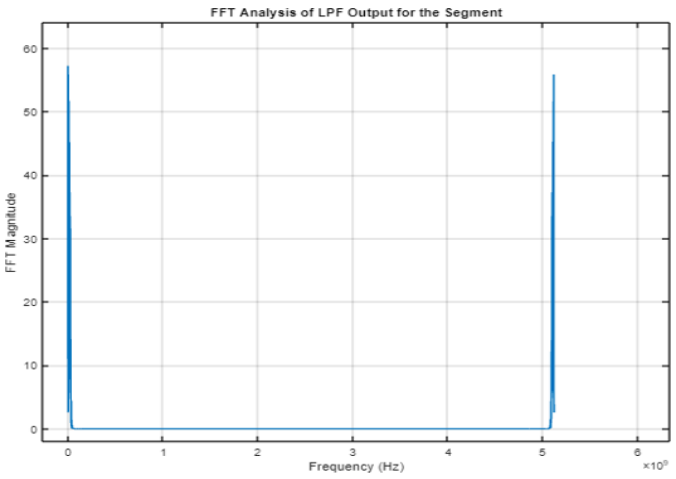

Figure 8 - FFT Analysis of Segmented 16-bit DAC Output

Fast Fourier Transform (FFT) analysis of a segmented 16-bit Digital-to-Analog Converter (DAC) involves examining the frequency domain characteristics of its output. In the segmentation approach, the DAC is divided into coarse and fine components to enhance resolution. During FFT analysis, the coarse and fine DAC outputs are individually subjected to frequency domain transformation. The resulting spectra reveal the distribution of signal energy across different frequencies. The coarse DAC FFT highlights the fundamental frequency and potential harmonic components, whilethefine DAC FFT provides additional detail in higher frequency regions. By analyzing these spectra, engineers gain insights into the DAC's performance, including its signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), and harmonic distortion. FFT analysis aids in optimizing the DAC design and assessing its suitability for applications requiring high precision, such as audio processing or telecommunications. The ability to scrutinize the frequency content of the segmented 16-bit DAC output through FFT analysis is instrumental in achieving a nuanced understanding of its performance characteristics and guiding furtherrefinements for optimal functionality.

Comparison of Sigma-delta DAC and segmented Sigma-delta DAC using MATLAB.

Parameters	SFDR (dB)	INL
Sigma-deltaDAC	87.6009 dB	0.50819
Segmented Sigma-deltaDAC	112.334 dB	0.5001

IV. CONCLUSION

In summary, the 16-bit Sigma-Delta DAC and the segmented 16-bit Sigma-Delta DAC both exhibit strengths and trade-offssuitable for various BIST applications. The conventional 16-bit Sigma-Delta DAC provides a simple and efficient solution for digital-to-analog conversion, while the segmented architecture leverages coarse and fine components to enhance resolution without compromising speed. The choice of DAC depends on the specific BIST requirements, considering factors like resolution and noise tolerance. The FFT analysis of the DAC outputs aids in assessing signal quality, and metrics like SNR, SFDR, and INL are crucial for evaluating their performance. Future work may involve further optimizing the segmented DAC and addressing calibration and real-time control aspects to maximize their utility in practical BIST systems.

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