

Design and Implementation of Adiabatic based Low Power Logic Circuits

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Abstract - *With the growing technology and markets demand necessitated the immediacy efforts in the field of development of low power VLSI design circuit. Though there are many approaches available that can be used to reduce the power/energy dissipation in conventional CMOS circuit which may include, reducing the supply voltage, or decreasing the node capacitances and minimizing the switching activities with efficient charge recovery logic. But all these reducing method have certain physical limitations, yet their limiting values are near but still they are in debatable. In this scenario many researchers are trying to adopt different optimization and energy conservation principle for VLSI circuit which led to the development of a new classical approach of switching logic known as adiabatic switching logic. The basic principle in adiabatic logic circuits is to slow down the logic transition varying from logic 1 to logic 0 and vice versa, aiming in reducing the power dissipation. Many different approaches/ techniques are proposed for implementing adiabatic logic circuits among which, PFAL is one of those techniques which positively promise assisting in the power issues. This paper present the simulation of NAND and NOR logic gate by CMOS and PFAL logic moreover with the help of simulated result by OrCAD PSPICE tool, it can be shown that the NAND & NOR used with adiabatic logic can reduce the power dissipation effectively than conventional CMOS circuit.*

Key Words: Low Power, Adiabatic Circuits, Logic Gates.

1. INTRODUCTION

With the cultivation of VLSI technology it had made possible, the integration of millions of transistor in lesser area which enabled more and more functionality but also led an increment in the power dissipation of the same chip.

As the technology is growing the need of portable devices is increased rapidly because of its convenience and essentiality of the social structure now days. The security system, surveillance system, wireless controls, RFID system, wireless sensor network, huge automatics system and others, are now becoming essential part of the society. The space industry also needs more and more compact ICs with as much as possible functionalities as the cost involved in it. Also the robustness of ICs is much more critical factor to make it qualify-able to be used.

Batteries are the essential part of portable devices but there advancement lag much far behind as compared to IC technology, therefore for compensating it certain necessary tradeoff are to be done. Moreover the increased demand for the low power chips and system comes from the environmental concerns as a recent survey shows that modern offices are now furnished with offices **automations equipment's that consumes large amount of power** [2,3].

Hence it is very important to concentrate on low power circuits rather than only high performances circuit, with the advancement of technology in last few years there is a dramatic shift in the approach of the industry researcher to come up with increased functionality and performances. Now the major dissipation in conventional CMOS circuit can be broadly classified as under two category i.e. static and dynamic power dissipation, which is caused mainly due to the current source, sub threshold MOS current, gate tunneling, capacitances, involved operation, speed, activity factor etc. The generalized power equation i.e.

$$P = C_{load} \cdot V_{dd}^2 \cdot f_{clk}$$

shows the average power dissipation can be reduce by altering certain parameter, but they also have certain limitation, therefore a new classical approach i.e. adiabatic switching logic which streamlined all those concept which try to reduce the power dissipation by increasing the time required for changing the voltage swings at various levels [4,7].

The adiabatic concepts is inherently taken from mechanical/ thermodynamics engineering which states "An adiabatic process is one in which no heat is gained or lost by the system". These circuits can be broadly classified as semi/ partial adiabatic and full /complete adiabatic circuits depending upon the level of Follow-ness

of the circuit w.r.t. the principles/ concepts laid down by the adiabatic logic approach. [1]

The paper is organized as follows: section 1 gives the brief introduction, Section 2 describes about adiabatic logic design and Section 3 describes the design methodology used to simulate the problem statement. In Section 4 we present the simulation results & discussion about them, finally Section 5 ends with conclusion and future work.

2. ADIABATIC LOGIC DESIGN

The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy [2].

It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not be possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems [5,6, 8,9].

Like many other adiabatic logic families, Reversible logic is a dual-rail logic family based upon a pair of cross-coupled inverters that are supplied using a power-clock, rather than a static DC power-supply. The configuration of the evaluation logic is what makes reversible logic an ideal family to implement fully reversible adiabatic logic [4]. This logic is constructed from nMOS devices attached between the power-clock and the outputs. These nMOS devices take complementary inputs and are constructed to produce a low-resistance path between the power-clock and the asserted output. The non-asserted output should be left with a high-impedance path to power-clock, and will be pulled low by the cross-coupled n-type devices. This means that the function is evaluated when there is sufficient differential between the two outputs, but far more importantly means that by using reverse-flowing data, the outputs can be more completely recovered. This should allow losses to be reduced to leakage [10, 11, 12,16].

3. IMPLEMENTATION & DESIGN

All the circuit are verified with several input combination, load capacitor (16fF), 5v sine wave in OrCAD PSPICE.

Positive Feedback Adiabatic Logic is a semi adiabatic approach which tries to increase the charging and discharging times maintaining the swing levels. It requires presence of dual nature of input (complemented and un-complemented) and creates dual nature for the output. Positive feedback adiabatic logic shows very positive aspects in addressing the power issues. [18-21]

PFAL comes in dual rail logic family which requires. Availability of both the complementary and Uncomplimentary inputs for the logic function. The Logic function (F) and (F bar) are implemented using NMOS networks alongside the two cross coupled inverters as latch known as sense amplifier which drives the two complementary outputs of the circuit. It consists of two PMOS and two NMOS switches which ultimately prevents the output terminals from degradation of logic levels. One of the logic blocks connects the concerned input to the power clock with a low resistance path and on the same time the other function provides a very high resistance in between the power clock and the other concerned output. **But the inverter's network provides the second output** a conducting path to the ground. In this way one of the two outputs different (either complementary or un-complementary one) is pulled up to the power clock and other down to the ground. [22, 23, 24]

PFAL use power clock instead of normal one as it is also used to energise the logic networks. That is no extra dc power used and a time varying ac signal is used to actuate the circuit elements along with the clocking control. In PFAL a 4 phase clock is used namely ideal, evaluate, hold recover stages. During evaluation phase the logic is evaluated as per the input vectors which is kept retained during the hold stage. The charge is recovered back during the recover stage. But PFAL does as partial recovery adiabatic logic family. The symbolic diagram of adiabatic gate is shown in fig 1.

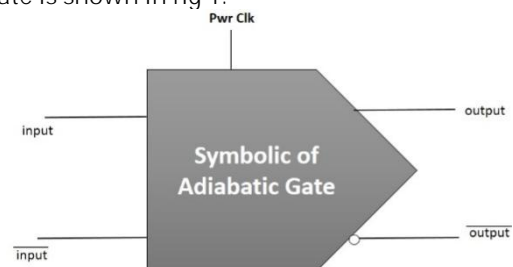


Fig 1: Symbolic diagram of adiabatic gate

3.1 Implementation of CMOS NAND Gate

Implementation of CMOS NAND gate will help us to analyze the power dissipation and compare it with the proposed adiabatic solution. The figure 2 shows the CMOS

NAND gate implementation in OrCAD PSPICE and fig 3 shows the layout of CMOS NAND gate in Microwind 3.1. The circuits of four MOS transistors. Figure 4 shows the input output waveforms of CMOS NAND gate whereas output power curve is shown in figure 5.

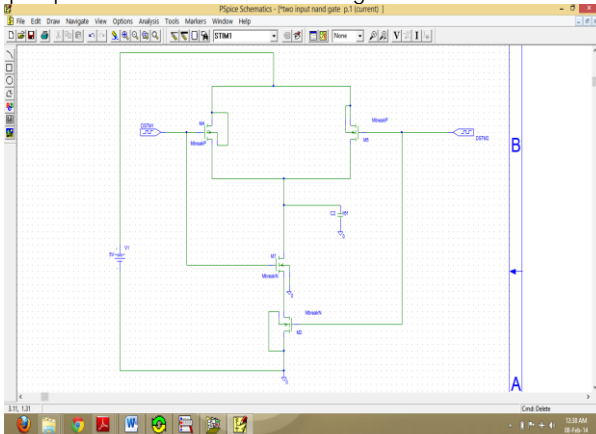


Fig 2: Simulated CMOS NAND gate

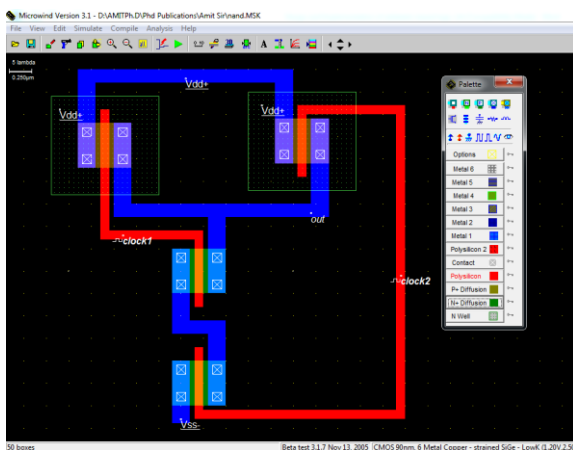


Fig 3: Layout of CMOS NAND



Fig4: Simulated input and output wave form of CMOS NAND gate (a) Input voltage $V_A = V_{DSTM1}$ & $V_B = V_{DSTM2}$ (b) Output voltage = $V(C2:2)$

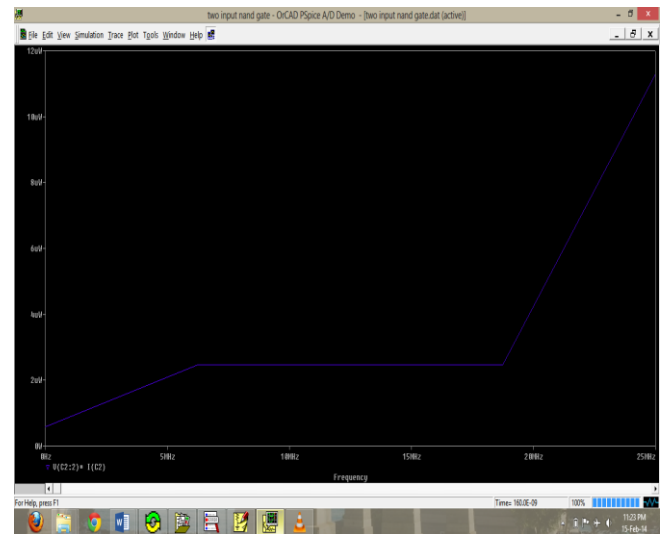


Fig 5: Output power curve for CMOS NAND gate

3.2 Simulation for a Two-Input PFAL NAND Gate

The figure 6 & 7 shows the PFAL NAND gate implementation in OrCAD PSPICE and Layout of PFAL NAND gate in Microwind 3.1. The circuits of four MOS transistors. Figure 8 shows the input output waveforms of PFAL NAND gate whereas output power curve is shown in figure 9. The design has been implemented with the help of 8 transistors which was 4 in case of CMOS design. The compromise of area has been balanced by the power reduction which varies from $1.1 \mu W$ to $2.4 \mu W$ instead of $1.1 \mu W$ to $10.8 \mu W$ in case of CMOS design. [25, 26]

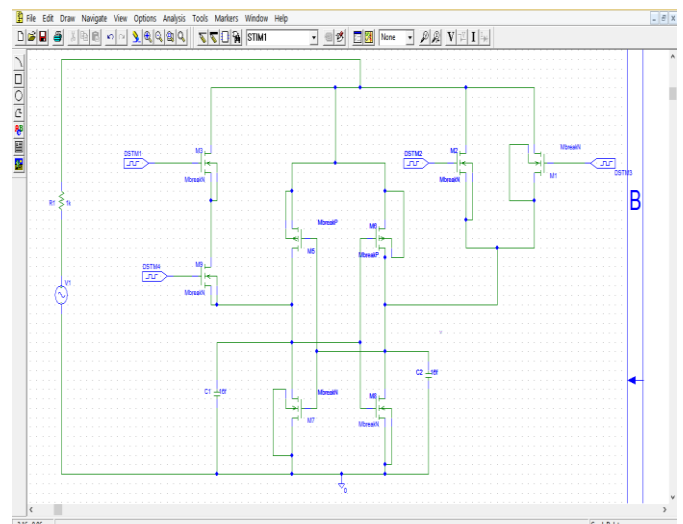


Fig 6: Simulated two inputs PFAL NAND gate

gate, Layout, its input output waveforms & output power curve.

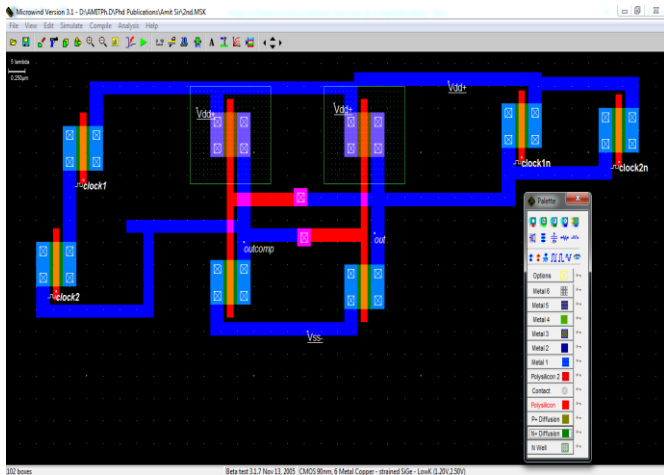


Fig 7: Layout of PFAL NAND Gate

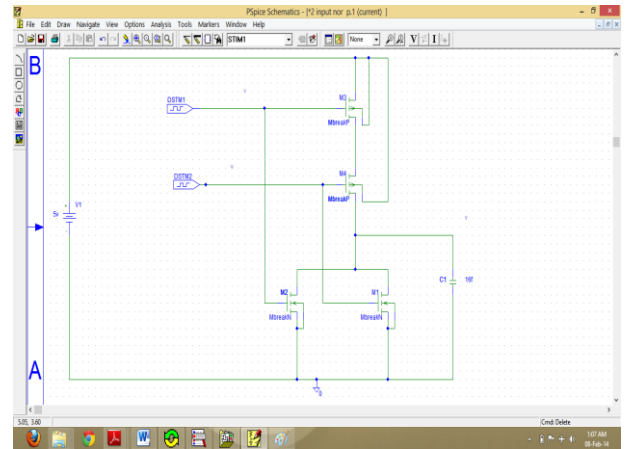


Fig 10: Simulated CMOS NOR gate

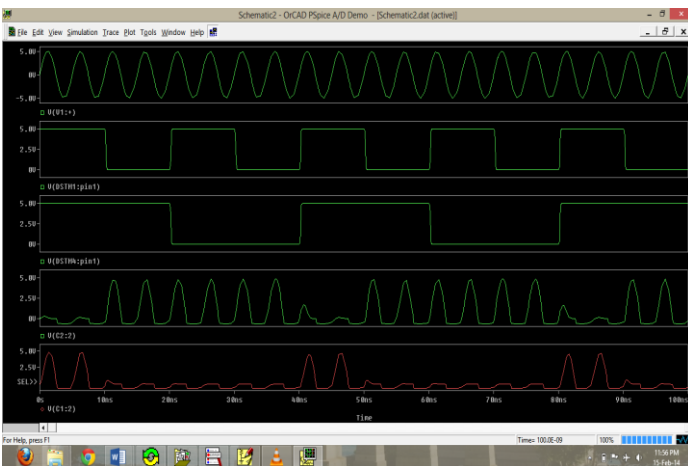


Fig 8: Simulated output waveform of PFAL NAND gate (a) Input VA=DSTM1 & VB =DSTM4 (b) output =V(C2:2)

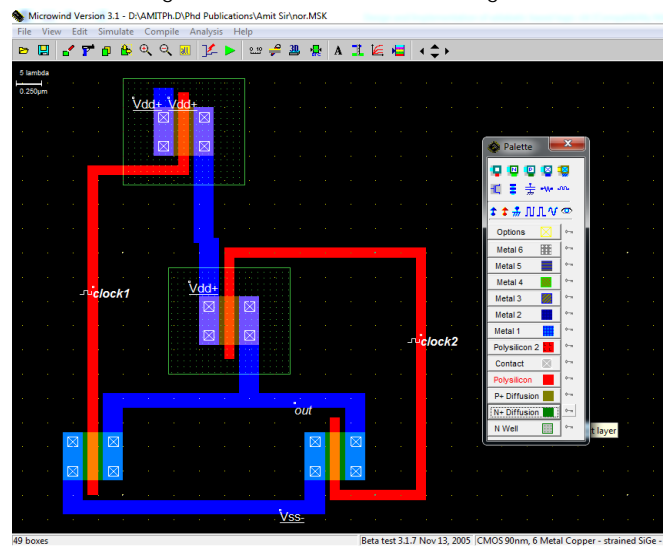


Fig 11: Layout of CMOS NOR Gate

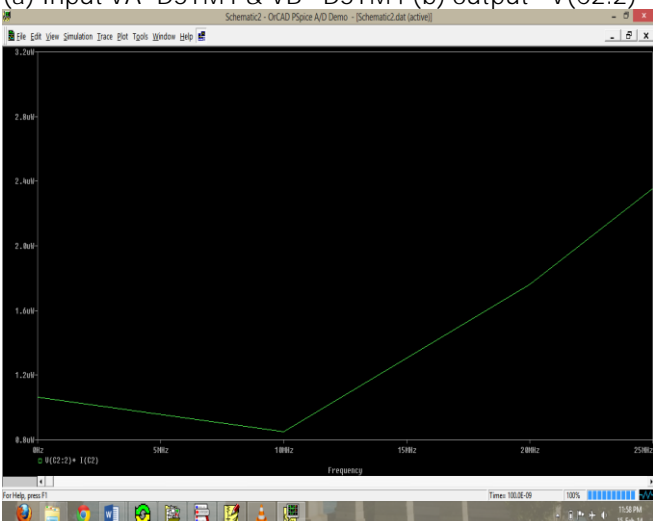


Fig 9: Output power curve for PFAL NAND gate

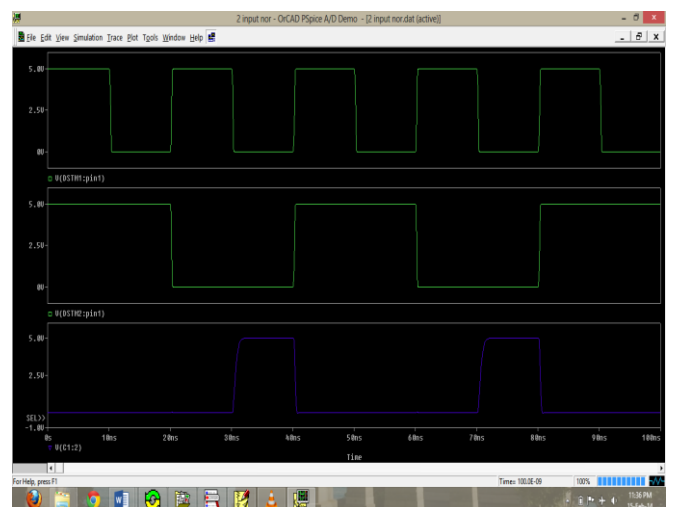


Fig 12: Simulated input and output waveform of CMOS NOR gate (a) Input VA=DSTM1 & VB =DSTM2 (b) Output =V(C1:2)

3.3 Simulation for a Two-Input CMOS NOR gate
 Implementing CMOS NOR gate using 4 transistor and comparing it with the PFAL NOR gate with 8 transistor. Figure 10, 11, 12 & 13 shows the schematic of CMOS NOR

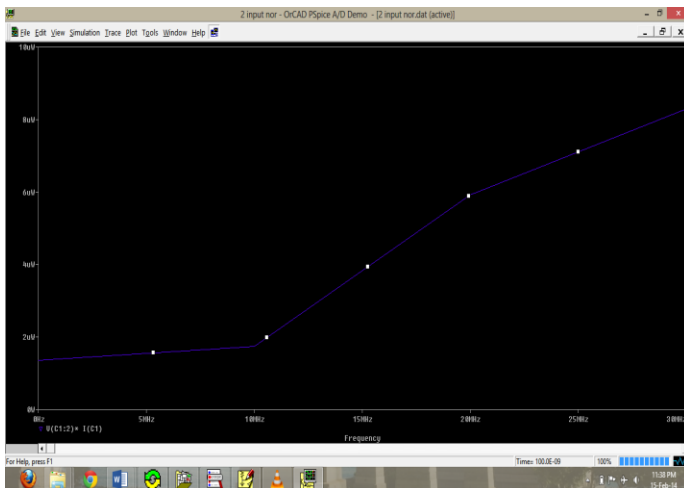


Fig 13: Output power curve for CMOS NOR gate

3.4 Simulation for a Two-Input PFAL NOR Gate

Implementing PFAL NOR gate using 8 transistor was done in OrCAD PSpice. Figure 14, 15 & 16 shows the schematic of PFAL NOR gate, its input output waveforms & output power curve.

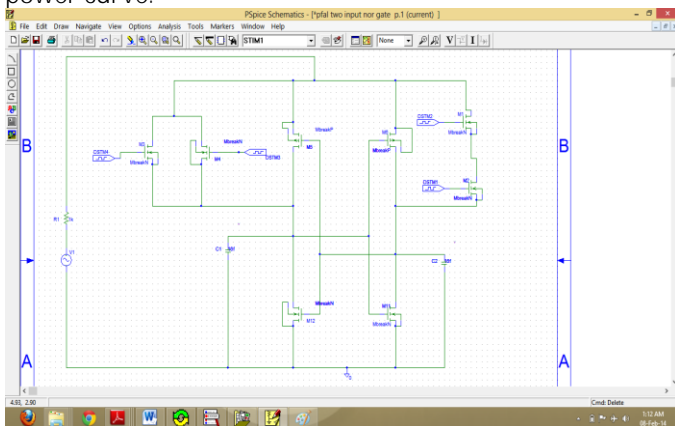


Fig 14: Simulated PFAL NOR gate

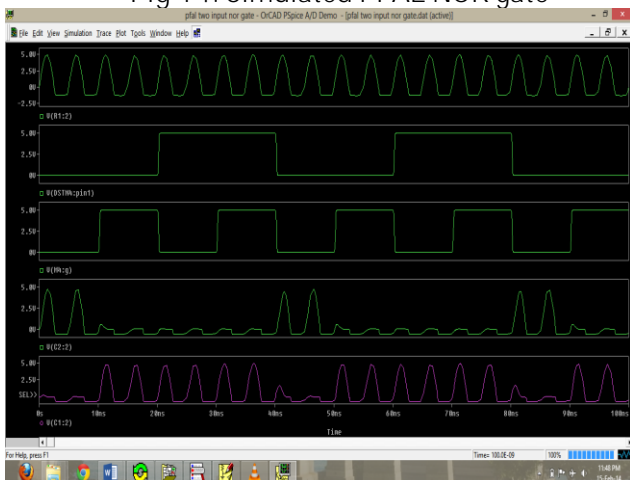


Fig 15: Simulated input and output wave form of CMOS NOR gate (a) Input VA=DSTM4& VB= DSTM3 (b)Output V(C2:2)

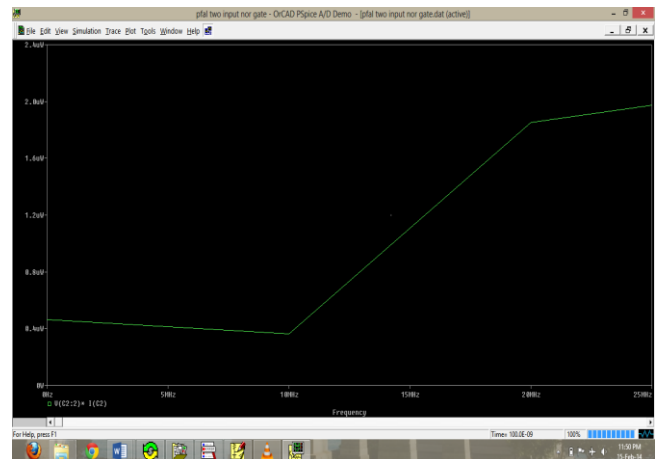


Fig 16: Output power curve for PFAL NOR gate

Comparison for Power & Area

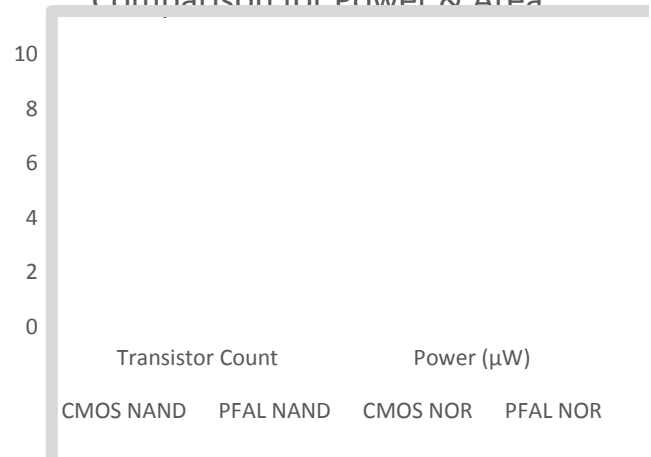


Fig 17: Comparison of CMOS based logic gate with PFAL based logic gates

4. CONCLUSION

Adiabatic circuits are low power solutions which will soon replace CMOS based logic circuits. From the above results, it is clearly depicted that adiabatic logic circuits reduce power dissipation with a design size penalty in terms of transistor count. Circuit simulations show that with the help of PFAL, the energy savings can be reached at a significant level. Utilizing the basic PFAL technology basic gates (NAND & NOR) are implemented, verified and analyzed. From the simulations the functionality of the implemented logic gates is found to be satisfactory.

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BIOGRAPHIES



Amit Saxena has 12 Years of experience in the field of Academic. He obtained his **Bachelor's degree in Electronics & Communication Engineering** from I.E.T., Rohilkhand University, Bareilly and Masters degree (VLSI Design) in 2008 from UPTU, Lucknow. He started his career from MIT, Moradabad. Presently he is working as an Assistant Professor, Deptt of E&C Engg., at MIT Moradabad. He has published number of papers in international & national journals, conferences and seminars. He is an active Member of Various Professional Societies such as ISTE, IACSIT, IAENG etc.



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